Hitachi Global Storage Technologies

Hard disk drive specifications

Hitachi Microdrive

with CF+ Type II interface

Models: DSCM-11000
DSCM-10512
DSCM-10340

Revision 4.0 13th January 2003

S07N-6022-09 Publication #7002

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1.0 General

This document describes the characteristics of 1.0-inch 3600-RPM hard disk drive with a CF+ Type II interface and with capacities of 1 GB, 512 MB, and 340 MB. This drive is the Hitachi Microdrive™ and is hereafter referred to as "the drive". This document defines the hardware functional and interface specifications. The drive is available in the following models:

- DSCM-11000
- DSCM-10512
- DSCM-10340

The major difference among DSCM-11000, DSCM-10512, and DSCM-10340 is the number of heads.

The specifications are subject to change without notice.

1.1 References

- Compact Flash Specification version 1.4
- Packaging
  - IBM packaging specification GA-21-9261-8
  - Packaging IBM Products, testing for shipment C-H 1-9711-005
- Electromagnetic Compatibility
  - IBM Corporate Standard C-S 2-0001-005
  - IBM Corporate Standard C-S 2-0001-012
  - IBM Corporate standard C-S 2-0001-026
  - IBM National Bulletin N-B 2-0001-401
  - IBM National Bulletin N-B 2-0001-403
  - IBM National Bulletin N-B 2-0001-308
- Safety
  - IBM Standard C-S 3-0501-070 (1991-10)
  - IBM Standard C-B 3-0501-950 IEC950
  - IBM Standard C-S 3-0501-951 UL1950
  - IBM Standard C-B 3-0501-952 CSA C22.2 No.950-M1995

1.2 Abbreviations

Kbpi	1,000 Bits Per Inch
Mbps	1,000,000 Bits per second
MB	1,048,576 bytes
KB	1,000 bytes
32 KB	32 x 1 024 bytes
64 KB	64 x 1 024 bytes
Mb/sq.in	1,000,000 bits per square inch
drive	DSCM-11000/-10512/-10340
Hitachi Microdrive™	DSCM-11000/-10512/-10340
MLC	Machine Level Control
TBD	to be defined

1.3 Drive handling precautions

- The drive can be easily damaged by shocks or Electric Static Discharge (ESD). Any damage incurred by the drive after removal of it from the shipping package and opening of the ESD protective bag is the user's responsibility.
- Do not apply pressing force onto the top or bottom surface of the drive.

DO NOT PRESS!

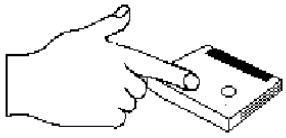
DO NOT PRESS WHEN REMOVING THE DRIVE

DO NOT PRESS WHEN CARRYING THE DRIVE

DO NOT APPLY PRESSURE WHEN ATTACHING THE DRIVE

- Do not seal the breather hole on the top cover.

DO NOT SEAL THIS HOLE!



SEALING THIS HOLE WILL RESULT IN LOSS OF DATA

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2.0 General features

- Compact Flash Type II Card Compliance
- 1024 MB, 512 MB and 340 MB formatted capacity
- 512 bytes/sector
- CF+ Type II Interface
- Integrated controller
- No-ID recording format
- E2PR 32/34 coding
- Multizone recording
- Enhanced ECC On-The-Fly
  - 40 bytes 3 way Interleaved Reed Solomon Code
  - 5 bytes per interleave On-The-Fly correction
- 128 KB (upper 68 KB is used for firmware) Segmented Buffer with write cache
- Fast data transfer rate
  - Up to 11.1 MB/sec for PIO mode
  - Up to 13.3 MB/sec for Multiword DMA mode (True IDE Mode only)
- Media data transfer rate 58.6 (outer zone) – 37.8 (inner zone) Mbit/s
- Average seek time 12 ms for read
- Closed-loop actuator servo (Embedded Sector Servo)
- True Track servo
- Rotary voice coil motor actuator
- Load/Unload mechanism
- Mechanical Latch
- Adaptive power save control (0.21 Watt at low power idle state)
- 1.5 sec Power on to ready
- Shock:
  - Nonoperating: 1500 G/1 ms
  - Operating: 175 G/2 ms

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Part 1. Functional specification

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3.0 Fixed disk subsystem description

3.1 Control electronics

The control electronics works with the following functions:

- Compact Flash Card Interface Protocol
- Embedded Sector Servo
- No-ID™ format
- Multi zone recording
- E2PR 32/34 Code
- ECC On-The-Fly
- Enhanced Adaptive Battery Life Extender

3.2 Head disk assembly

The following technologies are used in the drive:

- Pico slider
- Smooth glass disk
- GMR head
- Integrated Lead Suspension (ILS)
- Load/Unload mechanism
- Mechanical latch
- Corner bumper

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4.0 Fixed disk characteristics

4.1 Formatted capacity

The defaults of the logical drive parameters in Identify Device Data are as follows:

Description	DSCM-11000	DSCM-10512	DSCM-10340
Physical Layout			
Bytes per Sector	512	512	512
Sectors per Track	108–180	108–180	108–180
Number of Heads	2	1	1
Number of Disks	1	1	1
RPM	3600	3600	3600
Logical Layout			
Number of Heads	16	16	16
Number of Sectors/Track	63	63	63
Number of Cylinders	2088	1044	695
Number of Sectors	2,104,704	1,052,352	701,568
Total Logical Data Bytes	1,077,608,448	538,804,224	358,686,720

Figure 1. Formatted capacity

4.2 Data sheet

Rotational Speed (RPM)	3600
Data transfer rates (buffer to/from media)	37.8–58.6 Mb/s
Data transfer rates (host to/from buffer)	11.1 MB/sec (PIO mode3) 13.3 MB/sec (Multiword DMA mode1) at TRUE IDE
Recording Density (kBPI)	419 (Max)
Track Density (kTPI)	35
Areal Density (Gbits/sq-in)	14.6 (Max)
Data Bands	12

Figure 2. Data sheet

4.3 Performance characteristics

Drive performance is determined by the following parameters:

- Command overhead
- Mechanical positioning
  - Seek time
  - Latency
- Data transfer speed
- Buffering operation (Look ahead/Write cache)

Note: All the above parameters contribute to drive performance. Other parameters also contribute to the performance of the actual system. This specification describes only the characteristics of the drive, not the system throughput which depends on the system and the application.

The following table gives a typical value of each parameter. Detailed descriptions follow in the next sections.

Function	Typical
Average Random Seek Time for Read	12 ms
Average Random Seek Time for Write	13 ms
Rotational speed	3600 RPM
Power On To Ready	1.5 sec
Command Overhead	1 ms
Disk-buffer data transfer	37.8–58.6 Mbit/s
Disk-host data transfer	Refer to CFA Specification

Figure 3. Performance parameters

4.3.1 Command overhead

Command overhead time is defined as the total time from the receipt of the command by the drive to the start of motion of the actuator.

4.3.2 Mechanical positioning

4.3.2.1 Average Seek Time (Including Settling)

Command Type	**Typical** (ms)	**Max** (ms)
Read	12	14
Write	13	15

Figure 4. Mechanical positioning performance

Headings "**Typical**" and "**Max**" are given throughout the performance specification. **Typical** means the average of the drive population tested at nominal environmental and voltage conditions. **Max** means the maximum value measured on any one drive over the full range of the environmental and voltage

conditions. (See Section 7.1, “Environment” on page 21. See also Section 7.2, “DC Power Requirements” on page 23.)

The seek time is period of time from the start of the motion of the actuator to the start of a reliable read or write operation. A reliable read or write implies that error correction/recovery is not employed to correct arrival problems. The Average Seek Time is a measure of the weighted average of all possible seek combinations.

$$\text{Weighted Average} = \frac{\sum_{n=1}^{max} (max + 1 - n)(Tn_{in} + Tn_{out})}{(max + 1)(max)}$$

Where: max = Maximum Seek Length
n = Seek Length (1 to max)
Tn_{in} = Inward measured seek time for an n track seek
Tn_{out} = Outward measured seek time for an n track seek

4.3.2.2 Full Stroke Seek Time

Function	**Typical** (ms)	**Maximum** (ms)
Read	19.0	20.0
Write	20.0	21.0

Figure 5. Full stroke seek time

Full stroke seek is measured as the average of 1000 full stroke seeks.

4.3.2.3 Single Track Seek Time (without Command Overhead, including settling)

Function	**Typical** (ms)	**Maximum** (ms)
Read	2.0	3.0
Write	3.0	4.0

Figure 6. Single track seek time

Single track seek time is an average. The single track seek time is calculated by adding the time of inward and outward seek time of each single track and dividing that sum by the total number of tracks.

4.3.2.4 Average latency

Rotation speed (RPM)	**Time for a revolution** (ms)	**Average latency** (ms)
3600	16.7	8.3

Figure 7. Latency Time

4.3.2.5 Drive Ready Time/Mode Transition Time

Condition	Typical (sec)	Maximum (sec)
Power on to Stand by	0.5	0.7
Stand by to Idle	0.5	0.7

Figure 8. Drive Ready Time

4.3.3 Operating modes

Operating mode	Description
Spin-up	Start up time period from spindle stop or power down
Seek	Seek operation mode
Write	Write operation mode
Read	Read operation mode
Performance Idle	The drive is capable of responding immediately to media access requests. All electronic components remain powered and full frequency servo remains operational.
Active idle	Not used
Low power idle	Spindle motor is rotating normally with actuator unloaded to the parking positions.
Standby	The drive interface is capable of accepting commands. Spindle motor is stopped. All circuitry except the host interface is in power saving mode. The execution of commands is delayed until spindle becomes ready.
Sleep	Same as Standby

Figure 9. Operating modes

4.3.3.1 Operating mode at power on

The drive goes to Standby mode after Power On or Hard Reset as an initial state.

4.3.3.2 Adaptive Power Save Control

The transition timing from Performance Idle to Standby is adaptively and automatically controlled with the access pattern of the host system.

5.0 Data integrity

5.1 Data loss at power off

- Power off during any operations except for write operation will not cause any data loss.
- Power off during a write operation causes the loss of data received by the drive but not yet written onto the disk media.
- There is a possibility that power off during a write operation might make a maximum of 1 sector of data unreadable. This state can be recovered by a rewrite operation.

5.2 Write cache

- When write cache is enabled, there is a possibility that the write command completes before the actual disk write operation finishes. This means that there is a possibility that a power off event may occur even after a full write command finishes. This means that it is possible that even after a write command completion a power off might cause the loss of the data which the drive has received but not yet written onto the disk.
- In order to prevent data loss, confirm the completion of the actual write operation prior to the power off by issuing the Standby Immediate or Sleep command and confirming its completion.
- The default state of the write cache at power-on is "OFF."

5.3 Equipment status

Equipment status is available to the host system any time the drive is not ready to read, write, or seek. This status normally exists at power-on time and will be maintained until the following conditions are satisfied:

- Access recalibration/tuning is complete.
- Spindle speed meets requirements for reliable operation.
- Self-check of drive is complete.

Appropriate error status is made available to the host system if either of the following conditions occur after the drive has once become ready:

- Spindle speed outside requirements for reliable operation.
- Occurrence of a Write Fault condition.

5.4 WRITE safety

The drive ensures that the data is written onto the disk media properly. The following conditions are monitored during a write operation. When one of those conditions exceeds the criteria, the write operation is terminated and automatic retry sequence will be invoked.

- Head off track
- External shock
- Low supply voltage
- Spindle speed tolerance
- Head open/short

5.5 Data buffer test

The data buffer is tested at Power-on-reset. The test consists of a write/read "00"x and "ff"x pattern on each buffer position.

5.6 Error recovery

Errors occurring on the drive are handled by the error recovery procedure.

Errors that are uncorrectable after application of the error recovery procedures are reported to the host system as nonrecoverable errors.

5.7 Automatic reallocation

The sectors those show some errors may be reallocated automatically when specific conditions are met. The drive does not report automatic reallocation to the host system. The conditions for automatic reallocation are described below.

5.7.1 Nonrecovered write errors

When a write operation cannot be completed after the Error Recovery Procedure (ERP) is fully carried out, the sector(s) are reallocated to the spare location. An error is reported to the host system only when the write cache is disabled and the auto reallocation has failed.

5.7.2 Nonrecovered read errors

When a read operation has failed after defined ERP is fully carried out, a hard error is reported to the host system. This location is registered internally as a candidate for the reallocation. When a registered location is specified as a target of a write operation, a sequence of media verification is performed automatically. When the result of this verification meets the criteria, this sector is reallocated.

5.7.3 Recovered read errors

When a read operation for a sector fails once and is then recovered at the specific ERP step, this sector is reallocated automatically. A media verification sequence may be run prior to the reallocation according to the predefined conditions.

5.8 ECC

A 40-byte three-interleaved ECC processor provides user data verification and correction capability. The first four bytes of ECC are check bytes for user data and the other 36 bytes are Read Solomon ECC bytes. Each interleave has 12 bytes for ECC. Hardware logic corrects up to 15 bytes (5 bytes for each interleave) errors On-the-fly.

Following are examples of some error cases. "O" show that this byte contains no error. "X" shows that at least one bit of this byte is bad.

On The Fly correctable

Byte #	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	Error byte # for each interleave		
Interleave	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C
Error pattern	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	O	O	O	5	5	5
Error pattern	X	X	X	X	X	X	X	X	X	O	O	O	X	X	X	X	X	X	5	5	5

Uncorrectable

Byte #	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	Error byte # for each interleave		
Interleave	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C
Error pattern	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	O	O	6	5	5
Error pattern	X	O	O	X	O	O	X	O	O	X	O	O	X	O	O	X	O	O	6	0	0

Figure 10. ECC

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6.0 File organization

The following figure shows the cylinder allocation for the drive.

Zone	Cylinder	Sectors per Track
0	0–895	180
1	896–1791	180
2	1792–2431	165
3	2432–3327	154
4	3328–3839	150
5	3840–4223	144
6	4224–4607	140
7	4608–5375	135
8	5376–5759	126
9	5760–6399	120
10	6400–6911	112
11	6912–7167	108

Figure 11. Cylinder allocation

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7.0 Specification

7.1 Environment

7.1.1 Temperature and humidity

Operating conditions	
Temperature	0–55°C (ambient) (See Note)
Relative humidity	8–90%, non condensing
Maximum wet bulb temperature	29.4°C non condensing
Maximum temperature gradient	20°C/Hour
Altitude	–300 to 3048 m
Nonoperating conditions	
Temperature	–40 to 65°C (See note)
Relative humidity	5–95%, non condensing
Maximum wet bulb temperature	40°C, non condensing
Maximum temperature gradient	20°C/Hour
Altitude	–300 to 12,192 m

Figure 12. Temperature and humidity specifications

Note: Regardless of the ambient temperature, the drive can be operated at a maximum temperature of 65°C at the center of the base spindle of the drive.

The maximum storage period in the shipping package is one year.

7.1.1.1 Corrosion test

The hard disk drive must be functional and show no signs of corrosion after being subjected to temperatures of 50°C with 90% relative humidity for one week of storage followed by a return to 25°C with 40% relative humidity in two hours.

7.1.2 Radiation noise

The disk drive must work without degradation of the soft error rate under the following magnetic flux density limit at the enclosure surface.

Frequency	Limits (Gauss RMS)
0–60	5
61–100	2.5
101–200	1
201–400	0.5

Figure 13. Radiation noise

7.1.3 Conductive noise

The drive shall work without degradation of the soft error rate with an AC current of up to 45 mA(p-p) in the frequency range from DC to 20 MHz, injected through any two of the mounting screw holes of the drive via a 50-Ohm resistor.

7.1.4 Magnetic fields

The drive must withstand the radiation and conductive noise limits shown above. The test method is defined in the document "Noise Susceptibility Method" specification (P/N 95F3944).

7.2 DC power requirements

Connection to the drive should be made in a safety extra low voltage (SELV) circuit.

Power supply	+3.3V power supply case	+5V power supply case	Notes
Nominal supply	+3.3 Volts	+5 Volt	
Power supply ripple (0-20Mhz)	70 mV p-p max.	100 mV p-p max.	1
Tolerance	±5%	±5%	2
Supply current (nominal condition)	Population mean	Population mean	
Performance idle average	150 mA	170 mA	3
Low power idle average	65 mA	84 mA	
Read	220 mA	230 mA	4
Write	250 mA	260 mA	
Seek average	200 mA	215 mA	5
Standby	20 mA	20 mA	
Startup (maximum RMS in 10 ms windows)	200 mA	200 mA	6

Notes

1. The maximum fixed disk ripple is measured at 3.3 / 5 V input of the drive.
2. The drive shall not incur damage for an over voltage condition of +25% (maximum duration of 20 ms) on the 3.3 / 5 Volt nominal supply.
3. The idle current is specified at an inner track.
4. The read/write current is specified based on three operations of 63 sector read/write per 100 ms.
5. The seek average current is specified based on three operations per 100 ms.
6. The worst case operating current includes motor surge.

Figure 14. DC power requirements.

7.3 Reliability

7.3.1 Load/unload cycles

The drive will meet the specified error rates after the following Load/Unload cycles:

- 300,000 cycles (Load/Unload to be controlled by the drive microcode)
- 20,000 cycles (Emergency unloads)

7.3.2 Warranty

The warranty will be covered by contracts.

7.3.3 Life

To be discussed separately.

7.3.4 Preventive maintenance

None required.

7.4 Error rates

Error rates fall into two categories:

- Recoverable errors
- Nonrecoverable errors

The following error rates assume that no attempts are made to read or write in areas already identified as being defective. The error rates are defined for the drive operating at the full range of environmental conditions and are shown in Section 7.1 “Environment” on page 21. The voltage limits are shown in Section 7.2, “DC Power Requirements” on page 23.

7.4.1 Recoverable errors

A recoverable error is defined as an operation that failed the first time but succeeded in recovering the error when the drive error recovery procedure was invoked. ECC On-The-Fly, which is always active, is transparent to the system and is not counted as a recoverable error.

A typical drive shall have no more than one recoverable error per 100 million bits transferred (1 in 10^8) when operated at nominal voltage and environmental condition. The typical disk drive error rate represents the geometric mean of the error rates of the total disk drive population. The size of the drive population is 50 drives or more.

Each drive in the population shall have no more than one recoverable error per 10 million bits transferred (1 in 10^7) when operated at full range of voltage and environmental conditions and the operating vibration levels stated in Section 7.6, “Vibration and Shock” on page 27.

7.4.2 Nonrecoverable errors

A nonrecoverable error is defined as an operation that failed and was not recovered by the fixed disk error recovery procedure. No drive has more than one nonrecoverable error per 10 trillion bits transferred (1 in 10^{13}) when operated at the full range of voltage and environmental conditions.

7.5 Mechanical specifications

7.5.1 Physical dimensions and weight

The following table lists the dimensions and weight of the Hitachi Microdrive.

Height (mm)	5.0 + 0.0/–0.1
Width (mm)	42.80±0.101
Length (mm)	36.40±0.15
Weight (grams)	16 Max. (typical)

Figure 15. Physical dimensions and weight

7.5.2 Mechanical dimensions

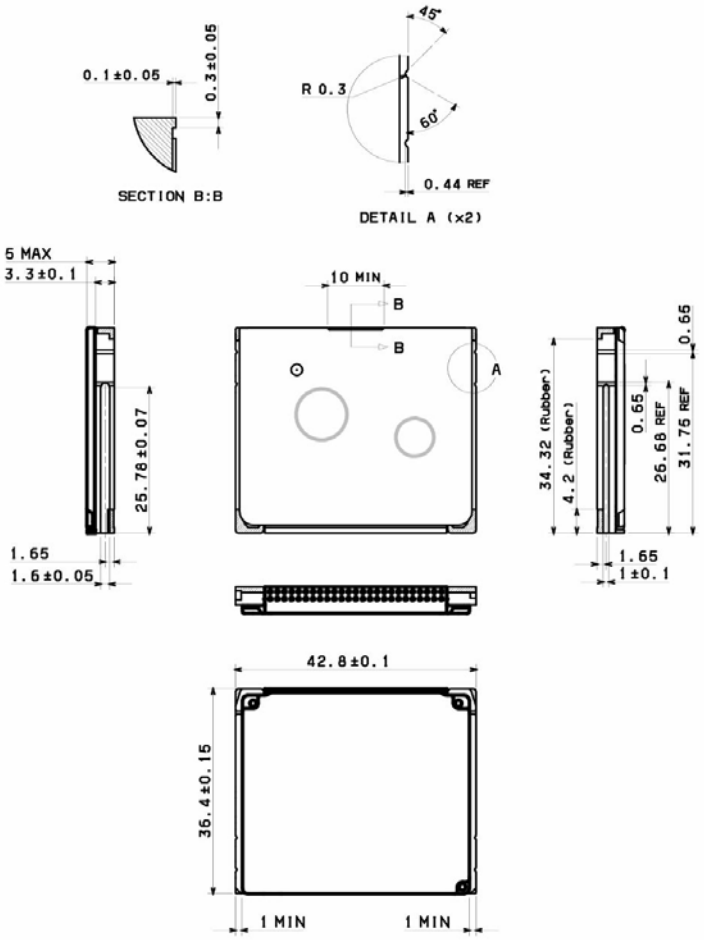


Figure 16. Mechanical outline of the drive

7.5.3 Connector

See Section 8.2, “Interface Connector” on page 33.

7.5.4 Mounting orientation

The drive will operate in all axes (360°).

Performance and error rate will stay within specification limits if the drive is operated in the other permissible orientations from which it was formatted. Thus a drive formatted in a horizontal orientation is able to run vertically and vice versa.

Vibration test and shock test are to be conducted by mounting the drive to the test table using a special fixture.

7.5.5 Load/Unload mechanism

The head load/unload mechanism is provided to protect the disk during shipping, movement, or storage. Upon power down, a head unload mechanism secures the heads at the unload position. See Section 7.6.4, “Nonoperating shock” on page 28 for additional details.

7.6 Vibration and shock

All vibration and shock measurements in this section are for the drive without the mounting attachments for the systems. The input level is applied to the normal drive mounting points.

7.6.1 Operating vibration

The drive will operate without a hard error while being subjected to the following vibration levels.

7.6.1.1 Operating random vibration

The test consits of 30 minutes of random vibration using the power spectral density (PSD) levels specified in C-S 1-9711-002 (1990-03) as V5L. The vibration test level for V5L is 0.67 G RMS.

Frequency (Hz)	g^2/Hz
5	$2.0 \times E^{-5}$
17	$1.1 \times E^{-3}$
45	$1.1 \times E^{-3}$
48	$8.0 \times E^{-3}$
62	$8.0 \times E^{-3}$
65	$1.0 \times E^{-3}$
150	$1.0 \times E^{-3}$
200	$5.0 \times E^{-4}$
500	$5.0 \times E^{-4}$

Note: Random vibration PSD profile breakpoints (Operating).

Figure 17. Random vibration

7.6.1.2 Operating swept sine vibration

- 1 G (Zero-to-peak), 5 to 500 to 5 Hz sine wave
- 2.0 oct/min sweep rate

7.6.2 Nonoperating vibration

7.6.2.1 Nonoperating random vibration

The test consists of a random vibration applied in each of three mutually perpendicular axes with a 15-minute duration per axis. The Power Spectral Density (PSD) levels for the test simulates the shipping and relocation environment which is shown below.

Frequency (Hz)	Power Spectral Density (g^2/Hz)
2.5	0.001
5	0.03
40	0.018
500	0.018

Note: Overall RMS level of vibration is 3.01 G RMS.

Figure 18. Random vibration PSD profile breakpoints (nonoperating)

7.6.2.2 Nonoperating swept sine vibration

- 5 G (zero-to-peak), 10 to 500 to 10 Hz sine wave
- 0.5 oct/min sweep rate

7.6.3 Operating shock

The drive meets the following criteria while operating under the conditions described as follows:

- The shock test consists of ten shock inputs in each axis and direction for a total of 60 shocks.
- There must be a minimum delay of 3 seconds between shock pulses. Soft errors and automatic retries are allowed during the test.
- No data loss or permanent damage occurs during a 175 G half-sine shock pulse of 2 ms duration and a 10-G half-sine shock pulse of 11 ms duration.
- The input level shall be applied to the normal disk drive subsystem mounting points of the device into which it is installed, as mounted in normal system use.

7.6.4 Nonoperating shock

The disk drive must withstand with no damage a 120 G half-sine wave shock pulse of 11 ms duration and a 1500 G half-sine wave shock pulse of 1 ms duration on six sides when heads are unloaded. (When the power is not applied to the unit, the heads are automatically located on the unloaded position.)

All shocks shall be applied in each direction of the drive's three mutually perpendicular axes, one axis at a time. Input levels shall be measured at the frame of the disk drive. The input level shall be applied to the device into which the Hitachi Microdrive is mounted. Through this device the operating shock is imparted to the Hitachi Microdrive through the normal disk drive guide rails and connector retention mountings of the device under test.

7.7 Acoustics

7.7.1 Sound power level

The criteria of A-weighted sound power level is described as follows.

Measurements are to be taken in accordance with ISO 7779. The mean of 40 drives is to be less than the typical value. Each drive is to be less than the maximum value. Drives are to meet this requirement in both board down orientations.

A-weighted sound power (Bels)	Typical	Maximum
Idle	2.1	2.4
Operating	2.2	2.5

Figure 19. Sound power levels

Background power levels of the acoustic test chamber for each octave band are to be recorded.

Sound power tests are to be conducted with the drive supported by spacers so that the lower surface of the drive is located at 25±3 mm height from the chamber floor. No sound absorbing material is used.

The acoustical characteristics of the disk drive are measured under the following conditions:

Mode definition

- **Idle mode**
  Power on, disks spinning, track following, unit ready to receive and respond to control line command
- **Operating mode**
  Continuous random cylinder selection and seek operation of actuator with a dwell time at each cylinder. Seek rate for the drive can be calculated as follows:

  Ns = 0.4 / (Tt + T1)

where

Ns = average seek rate in seeks/second
Tt = published seek time from one random track to another without including rotational latency
T1 = equivalent time, in seconds, for the drive to rotate by half a revolution

7.7.2 Discrete tone penalty

Discrete tone penalties are added to the A-weighted sound power (LW) with the following formula only when determining compliance:

LWt(spec) = LW + 0.1Pt + 0.3 < 4.0 (Bels)

where

LW = A-weighted sound power level
Pt = Value of discrete tone penalty [= dLt–6.0 (dBA)]
dLt = Tone-to-noise ratio taken in accordance with ISO 7779 at each octave band

7.8 Identification labels

The labels are affixed to every drive.

The top side of the label contains

- Model name
- Part number
- The statement "Made by IBM"
- Country of origin
- Notifications to the customer
- The marks of agencies approval
- Bar code of the serial numbers

The bottom side of the label contains

- The IBM logo
- The capacity
- The product name (Microdrive)

Due to space limitations, no additional requirements by customer are allowed.

7.9 Electromagnetic compatibility

The drive—when installed in a suitable enclosure and exercised with a random accessing routine at maximum data rate—meets the following worldwide EMC requirements.

- United States Federal Communications Commission (FCC) Rules and Regulations (Class B), Part 15
- RFI Suppression German National Requirements: IBM National Bulletin NB 2-0001-40
- RFI Japan VCCI Requirements of IBM products: IBM National Bulletin NB 2-001-403
- UE EMC Directive Technical Requirements and Conformity Assessment Procedures: NB 20-0001-038
- Electrostatic Discharge susceptibility limits for a class 2 ESD environment specified in IBM Corporate Standard C-S 2-0001-005andic
- Radiated Electromagnetic Susceptibility (RES) as specified in IBM Corporate Standard C-S 2-0001-012

IBM small LES development will provide technical support to assist users in complying with the EMC requirements.

7.9.1 CE Mark

The product is certified for compliance with EC directive 89/336/EEC. The EC marking for the certification appears on the drive.

7.9.2 C-Tick Mark

The product complies with the following Australian EMC standard—limits and methods of measurement of radio disturbance characteristics of information technology equipment per document AS/NZS 3548:1995 Class B,

7.10 Safety

7.10.1 Underwriters Lab (UL) approval

All models of the drive comply with UL 1950.

7.10.2 Canadian Standards Authority (CSA) approval

All models of the drive comply with CSA C22.2 950-M1995.

7.10.3 IEC compliance

All models of the drive comply with IEC 950.

7.10.4 German Safety Mark

All models of the drive are approved by TUV on Test Requirement EN 60 950:1988/A1:1990, but the GS mark has not been obtained.

7.10.5 Flammability

Printed circuit boards used in this product are made of material with a UL recognized flammability rating of V-1 or better. The flammability rating is marked or etched on the board. All other parts not considered electrical components except for minor mechanical parts are made of material with a UL recognized flammability rating of V-1 or better.

7.10.6 Safe handling

The products are designed for safe handling with regards to sharp edges and corners.

7.10.7 Environment

The product does not contain any known or suspected carcinogens.

Environmental controls meet or exceed all applicable government regulations in the country of origin. Safe chemical usage and manufacturing control are used to protect the environment. An environmental impact assessment has been done on the manufacturing process used to build the drive, the drive itself, and the disposal of the drive at the end of its life.

Production also meets the requirements of the international treaty on chloroflurocarbon (CFC) control known as the United Nations Environment Program Montreal Protocol, and as ratified by the member nations. Material to be controlled include CFC-11, CFC-12, CFC-113, CFC-114, CFC-115, Halon 1211, Halon 1301, and Halon 2402. Although not specified by the Protocol, CFC-112 is also controlled. In addition to the Protocol IBM requires the following:

- No packaging used for the shipment of the product uses controlled CFCs in the manufacturing process.

- No manufacturing processes for parts or assemblies—including printed circuit boards—use controlled CFC materials.

7.10.8 Secondary circuit protection

This product utilizes printed circuit wiring that must be protected against the possibility of sustained combustion due to circuit or component failures as defined in C-B 2-4700-034 (Protection Against Combustion). Adequate secondary over-current protection is the responsibility of the using system.

The user protects the DRIVE from its electrical short circuit problem. A 0.5-Amp limit is required for safety purposes.

7.11 Packaging

Drives are shipped in appropriate containers and placed on pallets in accordance with Hitachi Supplier Packaging Instruction (Hitachi specification GA-21-9261-8).

Drives procured under this specification are assembled and tested using "Electrostatic Discharge Protection" process and precedure—Hitachi document number EN/14/0116. A protection system suitable for the fixed disk drive must be installed and monitored by the appropriate ME/QA function. The goal is to prevent electrostatic potential from accumulating on any object which may deliberately or inadvertently be brought into contact with the drive.

Drives are shipped in ESD protective bags as defined in the Hitachi specification control drawing (P/N 6937283).

8.0 Electrical interface specifications

The following figure defines all the DC characteristics of the drive. Unless otherwise stated, the following are the electrical interface requirements:

- Vcc = 5 ± 5% V
- Vcc = 3.3 ± 5% V
- Ta = 0–55°C

(See Section 7.1, “Environment” on page 21)

Symbol	Item	Measurement method	Conditions	Units
V_{cc}	Input power	with respect to ground	–0.3 to 7.0	Volts
V_i	Input Voltage		–0.3 to V_{CC}+ 0.3	Volts
V_o	Output Voltage		–0.3 to V_{CC}+ 0.3	Volts
Pd	Power consumption	Ta = 25°C	1.2	Watt
T_{opr}	Operating Temperature		0–55	°C
T_{stg}	Storage temperature		–40 to 65	°C

Figure 20. DC characteristics

8.1 Cabling

Refer to CompactFlash specification.

8.2 Interface connector

The CompactFlash (CF) interface connector is designed to meet the connector interface specification specified in CF specification revision 1.4.

8.3 Signal definition

For the pin assignments of the interface signals, refer to the CompactFlash specification revision 1.4.

8.4 Signal description

Refer to Table 4-2 of CompactFlash specification revision 1.4 with the following exceptions:

- In True IDE Mode -INPACK (pin 43) is used as DMARQ (DMA request) for DMA data transfers. This signal is asserted by the device when it is ready to transfer data to or from the host.
- In True IDE Mode -REG (pin 44) is used as -DMACK (DMA acknowledge) for DMA data transfers. This signal is used by the host in response to DMARQ to initiate DMA transfers.

8.5 Interface logic signal levels

The interface logic signal has the following electrical specifications:

Symbol	Parameter	Condition		Minimum		Typical	Maximum		Unit
				3.135 V	4.75 V		3.465 V	5.25 V	
V_{OH}	"H" Output Voltage	I_{OH} = 2.0 mA (3.135V) 4.0mA (4.75V)	READY, INPACK#, BVDI, BVD2	3.00			3.45		Volts
		I_{OH} = 3.5 mA (3.135 V) 7.0 mA (4.75 V)	the other computer						
V_{OL}	"L" Output Voltage	I_{OH} = –2.5 mA (3.465V) –4.0 mA (5.25 V)	READY, INPACK#, BVDI, BVD2	–			0.4		Volts
		I_{OH} = –4.0 mA (3.465 V) –7.0 mA (5.25 V)	the other outputs						
I_{IH}	"H" Input Current	$V_{IN}=V_{CC}$	CE1#, CE2#, OE#, WE#, IORD#, IOWR#, REG#, CSEL, A10–A0	–1			1		mA
			RESET	63	90		70	110	
			BVD1, BVD2, D15–D0	–5			5		
I_{IL}	"L" Input Current	V_{IN} = GND PC Card Mode	CE1#, CE2#, OE#, WE#, REG#, IORD#, IOWR#, CSEL	–14	–20		–90	–140	mA
			RESET	–7	–10		–45	–70	
			A10–A0	–1			1		
			D15–D0	–5			5		
		V_{IN} = GND IDE Mode	CE1#, CE2#, IORD#, IOWR#, A10–A0, RESET	–1			1		
			D15–D0	–5			5		
			OE#, WE#, REG#, BVD1, BVD2, CSEL	–14	–20		–90	–140	

Figure 21. Interface logic signal levels

8.6 Attribute Memory Read timing

The Attribute Memory access time is defined as 300 ns. Detailed timing specifications are shown in the following two figures.

Symbol	Item	Minimum (ns)	Typical (ns)	Maximum (ns)
tcR	Read Cycle Time	300		
taA	Address Access Time			300
taCE	Card Enable Access Time			300
taOE	Output Enable Access Time			150
tdisCE	Output Disable Time from CE			100
tenOE	Output Enable Time from OE	5		
tvA	Data Valid from Address Change	0		
tsuA	Address Setup Time[1]	30		
thA	Address Hold Time[1]	20		
tsuCE	Card Enable Setup Time[1]	0		
thCE	Card Enable Hold Time[1]	20		
tvWT-OE	WAIT# Valid from OE[1]			35
twWT	WAIT# Pulse Width[2]			700
tvWT	Data Setup for WAIT# Released[2]	0		

1. These timing are specified for hosts and CF Cards which support the WAIT# signal.
2. These timings specified only when WAIT# is asserted within the cycle.

Figure 22. Attribute Memory Read timing data

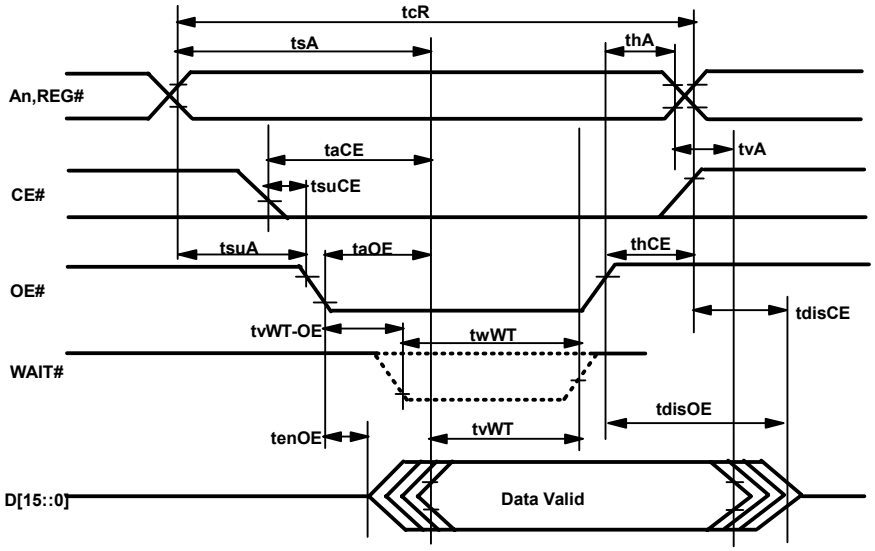


Figure 23. Attribute Memory Read timing diagram

8.7 Common Memory Read timing

Detailed timing specifications are shown in the following figure.

Symbol	Item	Minimum (ns)	Typical (ns)	Maximum (ns)
tcR	Read Cycle Time	250		
taA	Address Access Time			250
taCE	Card Enable Access Time			250
taOE	Output Enable Access Time			125
tdisCE	Output Disable Time from CE			100
tdisOE	Output Disable time from OE			100
tenCE	Output Enable Time from CE	5		
tenOE	Output Enable Time from OE	5		
tvA	Data Valid from Address Change	0		

Figure 24. Common Memory Read timing

8.8 Attribute and Common Memory Write timing

The Card Configuration write access time is defined as 250 ns. Detailed timing specifications are shown in the following figure.

Symbol	Item	Minimum (ns)	Typical (ns)	Maximum (ns)
tcW	Write Cycle Time	250		
twWE	Write Pulse Width	150		
taA	Address Setup Time	30		
tsuA-WEH	Address Setup Time for WE="H"	180		
tsuCE-WEH	Card Enable Setup time for	180		
tsuD-WEH	Data Setup Time for WE="H"	80		
thD	Data Hold Time	30		
trecWE	Write Recovery Time	30		
tdisWE	Output Disable Time from WE			100
tdisOE	Output Disable Time from OE			100
tenWE	Output Enable Time from WE	5		
tenOE	Output Enable Time from OE	5		
tsuOE-WE	Output Enable Setup for WE="H"	10		
thOE-WE	Output Enable Hold for WE="H"	10		

Figure 25. Attribute and Common Memory Write timing data

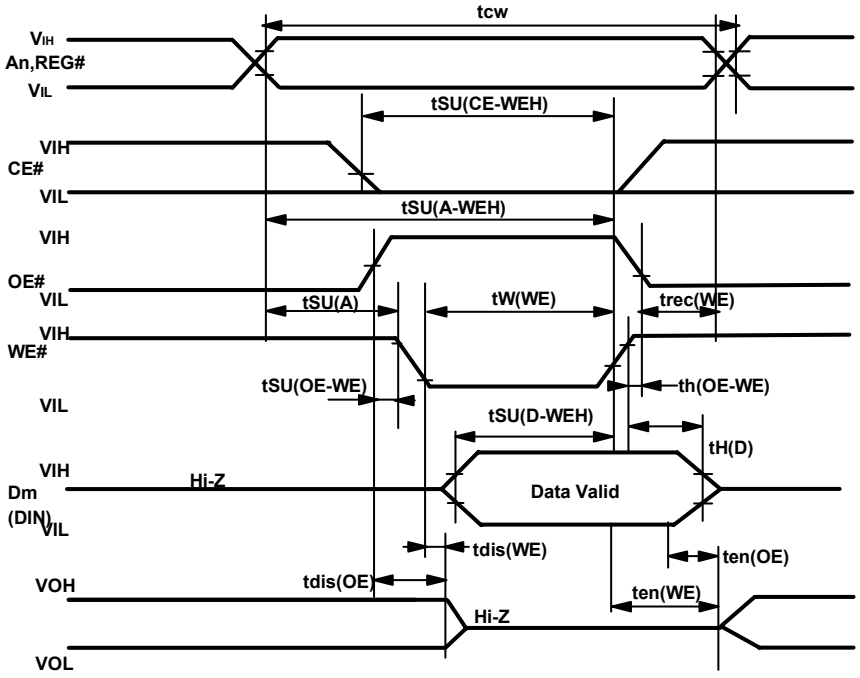


Figure 26. Attribute and Common Memory Write timing

8.9 I/O Input (Read) timing

Detailed timing specifications are shown in the following two figures.

Symbol	Item	Minimum (ns)	Maximum (ns)
td (IORD)	Data Delay after IORD		
tw			
th (IORD)	Data Hold following IORD	0	
tw (IORD)	IORD width Time	165	
tsu A (IORD)	Address Setup before IORD	70	
th A (IORD)	Address Hold following IORD	20	
tsu CE (IORD)	CE Setup before IORD	5	
th CE (IORD)	CE Hold following IORD	20	
tsu REG (IORD)	REG Setup before IORD	5	
th REG (IORD)	REG Hold following IORD	0	
tdf INPACK (IORD)	INPACK Delay Falling from IORD		45
tdr INPACK (IORD)	INPACK Delay Rising from IORD		45
tdf IOIS16 (ADR)	IOIS16 Delay Falling from Address		35
tdr iois16 (ADR)	IOIS16 Delay Rising from Address		35
tdf WT (IIORD)	Wait Deay Falling from IORD		35
tdr (WT)	Data Delay from Wait Rising		0
tw (WT)	Wait Width Time		350

Figure 27. I/O Input (Read) timing data

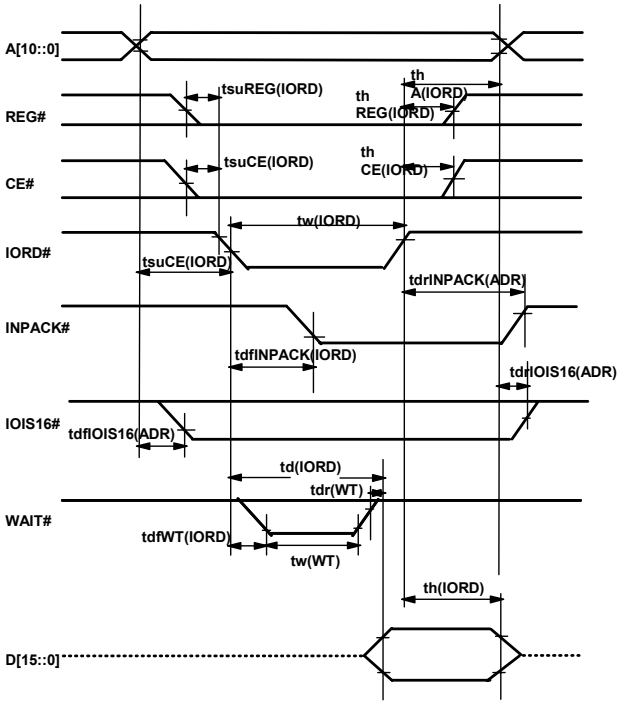


Figure 28. I/O Input (Read) timing diagram

8.10 I/O Output (Write) timing

Detailed timing specifications are shown in the following two figures.

Symbol	Item	Minimum (ns)	Maximum (ns)
td(IOWR)	Data Setup before IOWR	60	
th(IOWR)	Data Hold following IOWR	30	
tw(IOWR)	IOWR width Time	165	
tsuA(IOWR)	Address Setup before IOWR	70	
thA(IOWR)	Address Hold following IOWR	20	
tsuCE(IOWR)	CE Setup before IOWR	5	
thCE(IOWR)	CE Hold following IOWR	20	
tsuREG(IOWR)	REG Setup before IOWR	5	
thREG (IOWR)	REG Hold following IOWR	0	
tdf IOIS16 (ADR)	IOIS16 Delay Falling from Address		35
tdr IOIS16 (ADR)	IOIS16 Delay rising from Address		35
tdfWT(IOWR)	Wait Deay Falling from IOWR		35
tdr IOWR(WT)	IOWR high from Wait high	0	
tw(WT)	Wait Width Time		350

Figure 29. I/O Output (Write) timing data

Note: The maximum load on -WAIT, -INPACK, and -IOIS16 is 1LST TL with a 50 pF total load.

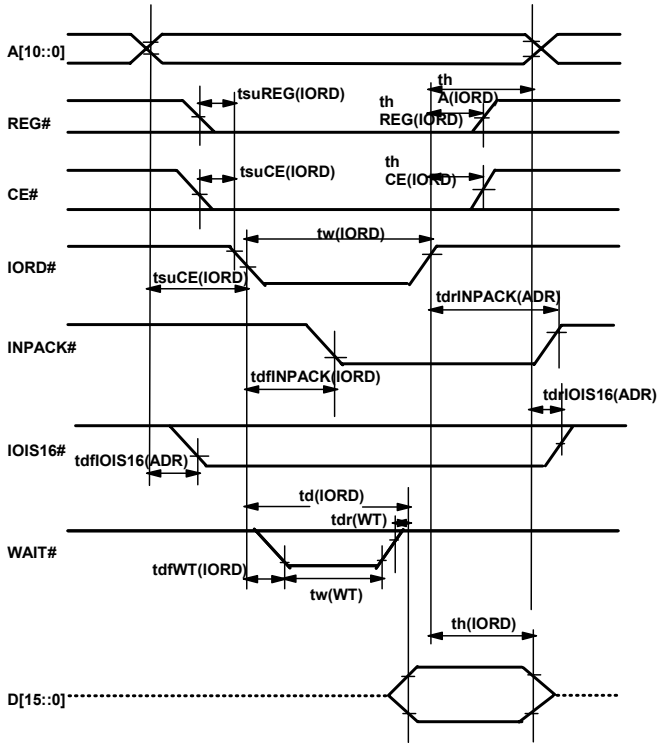


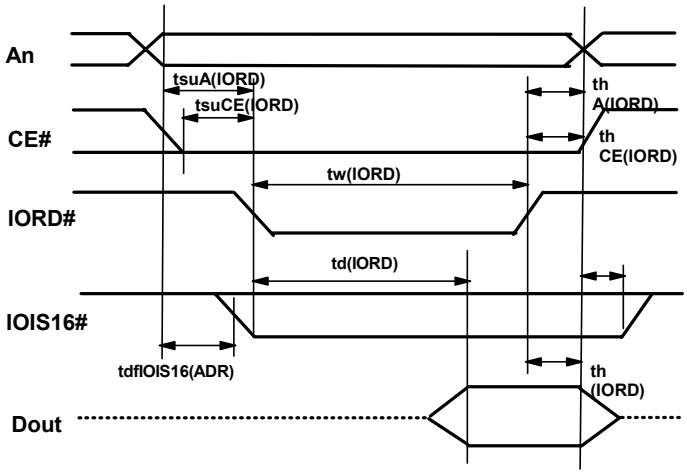
Figure 30. I/O Output (Write) timing diagram

8.11 True IDE Mode I/O Input (Read) Timing

Detailed timing specifications are shown in the following two figures.

Symbol	Item	Minimum (ns)	Maximum (ns)
td (IORD)	Data Delay after IORD		100
th (IORD)	Data Hold following IORD	0	
tw (IORD)	IORD Width Time	165	
tsu A (IORD)	Address Setup before IORD	70	
th A (IORD)	Address Hold following IORD	20	
tsu CE (IORD)	CE Setup before IORD	5	
th CE (IORD)	CE Hold following IORD	20	
tdf IOIS16 (ADR)	IOIS16 Delay Falling from Address		35
tdf IOIS16 (ADR)	IOIS16 Delay Rising from Address		35

Figure 31. True IDE Mode I/O Input (Read) timing data



Note: The maximum load on -IOIS16 is a 1 LSTTL with a 50 pF total load.

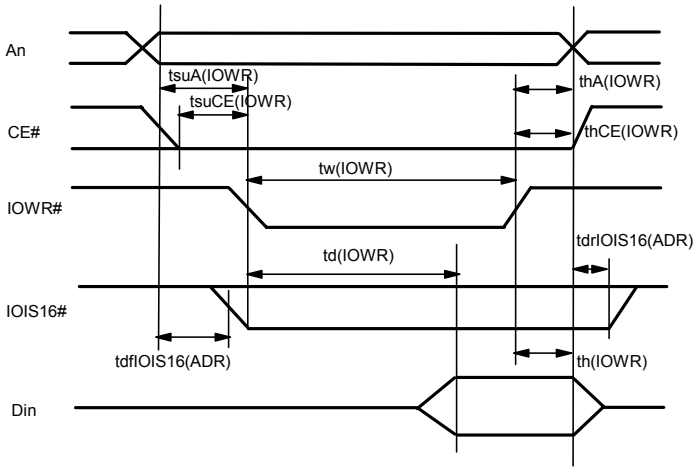
Figure 32. True IDE Mode I/O Input (Read) timing diagram

8.12 True IDE Mode I/O Output (Write) Timing

Detailed timing specifications are shown in the following two figures.

Symbol	Item	Minimum (ns)	Maximum (ns)
tsu(IOWR)	Data Setup before IOWR	60	
th(IOWR)	Data Hold following IOWR	30	
tw(IOWR)	IOWR Width Time	165	
tsuA(IOWR)	Address Setup before IOWR	70	
thA(IOWR)	Address Hold following IOWR	20	
tsuCE(IOWR)	CE Setup before IOWR	5	
thCE(IOWR)	CE Hold following IOWR	20	
tdfIOIS16(ADR)	IOIS16 Delay Falling from Address		35
tdrIOIS16(ADR)	IOIS16 Delay Riising from Address		35

Figure 33. True IDE Mode I/O Output (Write) timing data



Note: The maximum load on -IOIS16 is a 1 LSTTL with a 50 pF total load.

Figure 34. True IDE Mode I/O Output (Write) timing diagram

8.13 True IDE Mode Multiword DMA Data Transfer Timing

The device supports multiword DMA data transfer for Read DMA and Write DMA commands, which are available in true IDE mode only. In multiword DMA data transfer, INPACK# is used as DMARQ and REG# is used as DMACK#. Detailed timing specifications are shown in the following two figures. Note that the fastest transfer timing is equivalent to “DMA Mode 1” as defined in ATA/ATAPI-4 standard.

Symbol	Item	Minimum (ns)	Maximum (ns)
t0 (*1)	Cycle time	150	
tC	DMACK# to DMARQ delay		
tD (*1)	IOR#/IOW#	80	
tE	IOR# data access		60
tF	IOR# data hold	5	
tG	IOR#/IOW# data setup	30	
tH	IOW# data hold	15	
tI	DMACK# to IOR#/IOW# setup	0	
tJ	IOR#/DIOW# to DMACK# hold	5	
tKr (*1)	IOR# negated pulse width	50	
tKw (*1)	IOW# negated pulse width	50	
tLr	IOR# to DMARQ delay		40
tLw	IOW# to DMARQ delay		40
tZ	DMACK# to tristate		25

Notes:
(*1) t0 is the minimum total cycle time, tD is the minimum command active time, and tK (tKr or tKw, as appropriate) is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, tD, tK shall be met. The minimum tootle cycle time requirement, t0, is greater than the sum of tD and tK. This means the host can lengthen either tD or tK or both to ensure that t0 is equal to the value reported in the devices identify drive data.

Figure 35. Multiword DMA data transfer timing data

8.14 Power on/off timing

Detailed timing specifications are shown in the following two figures.

Symbol	Item	Condition	Minimum	Typ.	Max.	Units
		0 V =< V_{CC} < 2 V	0		V_{CC}	Volts
Vi(CE)	Card Enable signal level	2 V =< V_{CC} < V_{IH}	V_{CC}- 0.1	V_{CC}	V_{CC}+ 0.1	Volts
		V_{IH} =< V_{CC}	V_{IH}		V_{CC}+ 0.1	Volts
tsu(V_{CC})	Card Enable Setup time		20			ms
tsu (RESET)	RESET Setup time		20			ms
trec (Vcc)	Card Enable Recovery time		1			us
tpr	Power rising time	10% → 90% of V_{CC}	0.1		100	ms
tpf	Power falling time	90% of V_{CC} → 10%	3		300	ms
tw (RESET)	RESET pulse width		10			us
th (Hi-zRESET)			1			ms
ts (Hi-zRESET)			0			ms

Figure 36. Power On/Off timing data

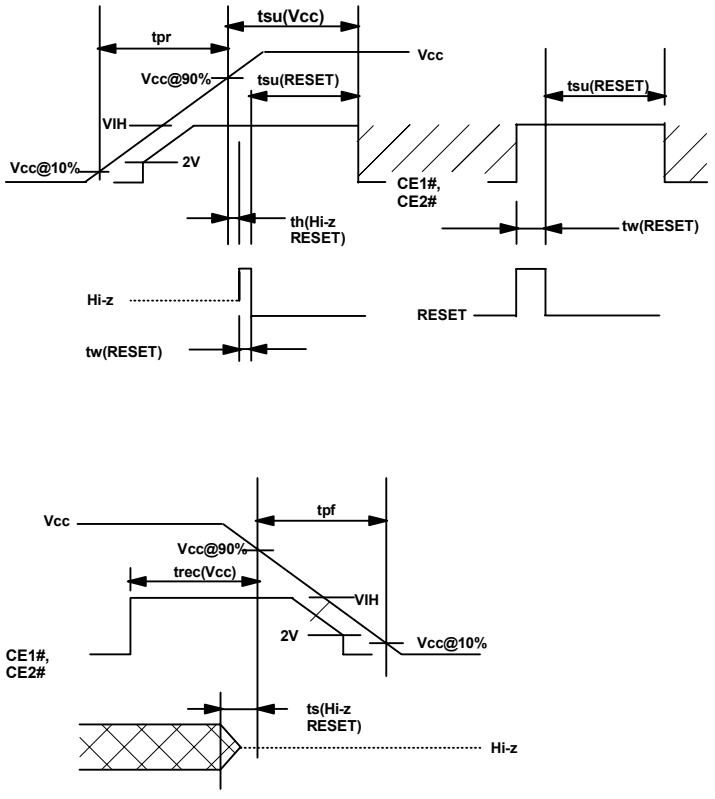


Figure 37. Power On/Off timing diagram

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Part 2. Interface specification

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9.0 General

9.1 Introduction

This specification describes the host interface of the DSCM-11000, -10512, -10340.

The interface conforms to the CF+ and CompactFlash specification with certain limitations described in Section 10.0, “Deviations from Standard.”

The drive supports the following new functions included in the CompactFlash specification 1.4 or newer:

- Format Unit Function
- ENABLE/DISABLE Delayed Write Function
- SENSE CONDITION command
- Metadata Storage Function

9.2 Terminology

Term	Meaning
Device	The DCSM-1xxxx hard disk drive
Host	The system to which the drive is attached
First Command	The first command which is executed after a power-on reset or a hard reset.
INTRQ	An interrupt request (either Device or Host)

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10.0 Deviations from Standard

Standby Timer Standby timer is enabled by STANDBY command or IDLE command. The value in the Sector Count register shall be used to determine the time programmed into the Standby timer. If the Sector Count register is zero, then the Standby timer is set to 109 minutes automatically.

Write Verify WRITE VERIFY command does not include read verification after write operation. The function is exactly same as WRITE SECTORS command.

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11.0 System interface

11.1 PCMCIA memory spaces and configuration registers

There are two types of memory address space in the drive: common memory and attribute memory. Common memory is the working address space used to map the memory arrays for storing data. It may be accessed by the host for memory read and write operations. The card permits both 8-bit and 16-bit accesses to all of its common memory addresses. Attribute memory is used for configuration information and is limited to 8-bit wide accesses only at even addresses. The attribute memory space contains the Card Information Structure (CIS) and configuration registers. The drive is identified by appropriate information in the CIS. The following configuration registers are used to coordinate the I/O specifications and the Interrupt level of cards that are located in the system.

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8–A4	A3	A2	A1	A0	Selected space
1	1	X	X	X	X	X	XX	X	X	X	X	Standby
X	0	0	0	1	0	1	XX	X	X	X	0	Configuration Registers Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8-bit D7–D0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8-bit D15–D8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16-bit D15–D0)
X	0	0	1	0	0	1	XX	X	X	X	0	Configuration Registers Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8-bit D7–D0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8-bit D15–D8)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (16-bit D15–D0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Read)
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Write)

Figure 38. Registers and memory space decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8–A4	A3	A2	A1	A0	Selected space
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Register Read
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Register Write
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write

Figure 39. Configuration registers decoding

11.2 Card configuration registers

The device has a set of configuration registers in attribute memory space. These registers are used to control the configurable characteristics of the card. The configurable characteristics include the electrical interface, I/O address space, interrupt request, and power requirements of the card. These registers also provide a method for accessing status information about the card. The information can be used to arbitrate between multiple-interrupt sources on the same interrupt request level. Addresses of the configuration registers are specified by the Configuration registers Base Address in the TPCC_RADR field of the CISTPL_CONFIG (16-bit PC Card Configuration Tuple) and offset relative to the base address. For example, the Configuration and Status register can be located at offset 02h from the base address. The addresses of the card configuration registers should always be read from the CIS since these addresses may vary in future products.

11.2.1 Configuration Option Register (Offset 00h)

The Configuration Option Register is used to configure the cards interface, address decoding, and interrupt and to issue a soft reset to the device.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevlREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

Figure 40. Configuration Option Register (Offset 00h)

SRESET: Soft Reset-Setting this bit to one (1), waiting for the minimum reset width time, and returning to zero (0) places the card in the Reset state. Setting this bit to one (1) is equivalent to the assertion of the +RESET signal except that the SRESET bit is not cleared. Returning this bit to zero (0) leaves the card in the same unconfigured Reset state as following power-up and hardware reset. This bit is set to zero (0) by power-up and hardware reset. Using PCMCIA Soft Reset is considered a hard reset from the ATA point of view. An ATA soft reset is issued through the Device Control Register.

LevlREQ: This bit is set to one (1) when level mode Interrupt is selected, and zero (0) when pulse mode is selected. Set to zero (0) by. This bit is set to zero (0) by power-up and hardware reset. When the card is in Level Mode, the –IREQ pin is pulled up to Vcc on the card and asserted low to signal an interrupt. The interrupt is kept asserted until the host reads the card status register, thereby resetting the interrupt indication and causing –IREQ to be deasserted. When the card is in pulse mode, the card signals an interrupt by the trailing edge of the negative pulse which width is at least 0.5 ms.

Conf5 - Conf0: Configuration Index. This is set to zero (0) by power-up and hardware reset. It is used to select operation mode of the card as shown below. Conf5 and Conf4 are reserved and must be written as zero (0).

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Card Configuration Mode
0	0	0	0	0	0	Memory mapped
0	0	0	0	0	1	I/O mapped 16 contiguous registers at any 16-byte system decoded boundary
0	0	0	0	1	0	Primary I/O mapped, 1F0h n 1F7h/3F6h n 3F7h
0	0	0	0	1	1	Secondary I/O mapped, 170h n 177h/376h n 377h

Figure 41. Configuration Index

11.2.2 Card Configuration Status Register (Offset 02h)

The Card Configuration and Status Register contains information about the card condition.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOis8	-XE	0	PwrDwn	Int	0
Write	0	SigChg	IOis8	-XE	0	PwrDwn	0	0

Figure 42. Card Configuration Status Register (Offset 02h)

Changed: This bit indicates that one or both of the Pin Replacement register CRdy, or CWProt bits are set to one (1). When the Changed bit is set, pin 46 (–STSCHG) is held low if the SigChg bit is a one (1) and the card is configured for the I/O interface.

SigChg: This bit serves as a gate for pin 46 (–STSCHG). If the card is configured for the I/O interface and this bit is zero (0), pin 46 (–STSCHG) is held high. If the card is configured for the I/O interface and both the Changed and SigChg bits are set to one (1), the card asserts pin 46 (–STSCHG) upon changes in the Changed bit.

IOis8: This bit is set to one (1) when the card is configured in 8-bit I/O mode as the host provides I/O cycles only with an 8-bit (D7–D0) data path.

-XE: Extended power enabled. When the host sets this bit to zero (0), the card enables extended power operations. When the host sets this field to one (1), the card disables extended power operations. When this filed is read, the bit indicates the card's acceptance of extended power operations. If it is read as one (1), extended power operations are being disabled. If it is read as zero (0), the card can perform extended power operations. This bit is read as zero (0) after power-up and hardware reset. Identify Device information word 170 also has –XE bit for the same purpose. These –XE bits are always consistent. Extended power operations are defined as a command that requires the extended power capability of the host. For the device, extended power operations includes any read, write and seek commands. Identify Device, Set Features (Enable Extended Power and Disable Extended Power), Request Sense and Execute Device Diagnostics are not extended power operations, that is, these commands can be performed regardless of the setting in –XE bit.

PwrDwn: This bit indicates whether the hosts requires the card to be in the power saving or active mode. When the bit is one (1), the card enters power down mode, which is the same mode the card enters upon a completion of SLEEP command. When the bit is zero (0), the card enters the active mode. The PCMCIA Rdy/-Bsy signal becomes BUSY when this bit is changed. Rdy/-Bsy will not become READY until the power sate requested has been entered. The device automatically powers down when it is idle and powers back up when it receives a command. Duration of active mode to power down mode is variable as determined by the Adaptive Battery Life Extender 3 (ABLE-3) technology.

Int: This bit represents the internal state of the interrupt request. This value is available whether or note I/O interface has been configured. This signal remains true until the condition which caused the interrupt request has been serviced. If interrupts are disabled byte –IEN bit in the Device Control Register, this bit is zero (0).

11.2.3 Pin Replacement Register (Offset 04h)

The Pin Replacement Register is used to provide the card status information about READY and WP.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CRdy/-Bsy	0	1	1	Rdy/-Bsy	0
Write	0	0	CRdy/-Bsy	0	0	0	MRdy/-Bsy	0

Figure 43. Pin Replacement Register (Offset 04h)

Crdy/-Bsy: This bit is set to one (1) when the bit Rdy/-Bsy changes state. This bit can also be written by the host.

Rdy/-Bsy: This bit is used to determine the internal state of the Rdy/-Bsy signal. This bit can be used to determine the state of the RDY/-BSY as this pin has been reallocated for use as –IREQ on the I/O interface.

MRdy/-Bsy: This bit acts as a mask for writing the corresponding bit CRdy/-Bsy.

11.2.4 Socket and Copy Register (Offset 06h)

This register contains additional configuration information. The host must always set this register before writing configuration index to the Configuration Option Register.

Operation	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Read	Reserved	0	0	Device #	0	0	0	0
Write	0	0	0	Device #	X	X	X	X

Figure 44. Socket and Copy Register (Offset 06h)

Reserved: This bit is reserved for future standards. This bit must be set to zero (0) by the host whenever the register is written.

Device #: This is always read as zero (0) and must be set to zero (0) as the device does not support twin card configuration.

X: the socket number field is ignored by the device.

11.3 CF-ATA Register Set Definition and Protocol

The drive can be configured as an I/O device through

- Primary I/O mapped address spaces (1F0h–1F7h, 3F6h–3F7h) or secondary I/O mapped address spaces (170h–177h, 376h–377h)
- Contiguous I/O mapped address spaces; any system decoded 16-byte I/O block
- Memory mapped space
- True IDE mode; only I/O operations to the Task File and Data registers allowed, no PCMCIA functionality.

The communication to or from the card is done using the Task File registers which provide all the necessary registers for control and status information.

11.3.1 Primary or Secondary I/O mapped addressing

-REG	A9–A4	A3	A2	A1	A0	-IORD=0	-IOWR=0	Notes
0	1Fh(17h)	0	0	0	0	Even RD Data	Even WR data	1,2
0	1Fh(17h)	0	0	0	1	Error Register	Features	1,2
0	1Fh(17h)	0	0	1	0	Sector Count	Sector Count	
0	1Fh(17h)	0	0	1	1	Sector Number	Sector Number	
0	1Fh(17h)	0	1	0	0	Cylinder Low	Cylinder Low	
0	1Fh(17h)	0	1	0	1	Cylinder High	Cylinder High	
0	1Fh(17h)	0	1	1	0	Device/Head	Device/Head	
0	1Fh(17h)	0	1	1	1	Status	Command	
0	1Fh(17h)	0	1	1	0	Alternate Status	Device Control	
0	1Fh(17h)	0	1	1	1	Device Address	Reserved	

Figure 45. Primary or Secondary I/O mapped addressing

Notes:
1. Register 0 is accessed with -CE1 low and -CE2 low (and A0 = don't care) as a word register on the combined Odd Data Bus and Even Data Bus (D15–D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. The address space of this word register overlaps the address space of the Error and Feature byte-wide register that lie at offset 1. When accessed twice as a byte register with -DE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.

2. A byte access to Register 0 with -CE1 hogh and -CE2 low accesses the error (read) or feature (write) register

11.3.2 Contiguous I/O mapped addressing

-REG	A3	A2	A1	A0	Offset	-IORD=0	-IOWR=0	Notes
0	0	0	0	0	0	Even RD Data	Even WR Data	1
0	0	0	0	1	1	Error	Features	2
0	0	0	1	0	2	Sector Count	Sector Count	
0	0	0	1	1	3	Sector Number	Sector Number	
0	0	1	0	0	4	Cylinder Low	Cylinder Low	
0	0	1	0	1	5	Cylinder High	Cylinder High	
0	0	1	1	0	6	Device/Head	Device/Head	
0	0	1	1	1	7	Status	Command	
0	1	0	0	0	8	Dup. Even RD Data	Dup. Even WR Data	2
0	1	0	0	1	9	Dup. Odd RD Date	Dup. Odd WR Data	2
0	1	1	0	1	D	Dup. Erorr	Dup. Features	2
0	1	1	1	0	E	Alternate Status	Device Control	
0	1	1	1	1	F	Device Address	Reserved	

Figure 46. Contiguous I/O mapped addressing

Notes:

1. Register 0 is accessed with -CE1 low and -CE2 low (and A0 = don't care) as a word register on the combined Odd Data Bus and Even Data Bus (D15–D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. The address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as a byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access. A byte access to register 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

2. Registers at offset 8, 9, and D are nonoverlapping duplicates of the registers at offset 0 and 1. Register 8 is equivalent to register 0, while register 9 accesses the odd byte. Therefore, if the registers are byte accessed in the order 9 and then 8 the data will be transferred by first the odd byte and then the even byte. Repeated byte accesses to register 8 or 0 will access consecutive (even then odd) bytes from the data buffer. Repeated word accesses to register 8, 9, or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte access to registers 8 and then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 accesses only the odd byte of the data.

3. Address lines that are not indicated are ignored by the device for accessing all the registers in this table.

11.3.3 Memory mapped addressing

-REG	A10	A9-A4	A3	A2	A1	A0	Offset	-OE=0	-WE=0	Notes
1	0	x	0	0	0	0	0	Even RD Data	Even WR Data	1,2
1	0	x	0	0	0	1	1	Error	Features	1,2
1	0	x	0	0	1	0	2	Sector Count	Sector Count	
1	0	x	0	0	1	1	3	Sector Number	Sector Number	
1	0	x	0	1	0	0	4	Cylinder Low	Cylinder Low	
1	0	x	0	1	0	1	5	Cylinder High	Cylinder High	
1	0	x	0	1	1	0	6	Device/Head	Device/Head	
1	0	x	0	1	1	1	7	Status	Command	
1	0	x	1	0	0	0	8	Dup. Even RD Data	Dup. Even WR Data	2
1	0	x	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
1	0	x	1	1	0	1	D	Dup. Error	Dup. Features	2,4
1	0	x	1	1	1	0	E	Alternate Status	Device Control	
1	0	x	1	1	1	1	F	Device Address	Reserved	
1	1	x	x	x	x	0	8	Even RD Data	Even WR Data	3
1	1	x	x	x	x	1	9	Odd RD Data	Odd WR Data	3

Figure 47. Contiguous I/O mapped addressing

Notes:

1. Register 0 is accessed with -CE1 low and -CE2 low as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access. A byte access to address 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

2. Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1. Register 8 is equivalent to register 0, while register 9 accesses the odd byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data will be transferred odd byte then even byte. Repeated byte accesses to register 8 or 0 will access consecutive (even then odd) bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.

3. Accesses to even addresses between 400h and 7FFh access register 8. Accesses to odd addresses between 400h and 7FFh access register 9. This 1 Kbyte memory window to the data register is provided so that hosts can perform memory to memory block moves to the data register when the register lies in memory space. Some hosts, such as the X86 processors, must increment both the source and destination addresses when executing the memory to memory block move instruction. Some PCMCIA socket adapters also have auto incrementing address logic embedded within them. This address window allows these hosts and adapters to function efficiently. Note that this entire window accesses the Data Register FIFO and does not allow random access to the data buffer within the Hitachi Microdrive. A word access to

address at offset 8 will provide even data on the low-order byte of the data bus, along with odd data at offset 9 on the high- order byte of the data bus.

4. The Hitachi Microdrive does not support accessing the Dup. Features and the Dup. Error as word register at offset 0Ch with CE1 low and CE2 low.

11.3.4 True IDE Mode addressing

-CE2	-CE1	A2	A1	A0	-IORD=0	-IOWR=0
1	0	0	0	0	RD Data	WR Data
1	0	0	0	1	Error	Features
1	0	0	1	0	Sector Count	Sector Count
1	0	0	1	1	Sector Number	Sector Number
1	0	1	0	0	Cylinder Low	Cylinder Low
1	0	1	0	1	Cylinder High	Cylinder High
1	0	1	1	0	Device/Head	Device/Head
1	0	1	1	1	Status	Command
0	1	1	1	0	Alternate Status	Device Control
0	1	1	1	1	Device Address	Reserved

Figure 48. True IDE Mode addressing

The Command Block Registers are used for sending commands to the device or for posting status from the device.

The Control Block Registers are used for device control and for posting alternate status.

11.4 CF-ATA Registers

11.4.1 Alternate Status Register

Alternate Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR

Figure 49. Alternate Status Register

This register contains the same information as the Status Register. The only difference is that reading this register does not imply interrupt acknowledge or clear a pending interrupt. See Section 11.4.13, "Status Register" on page 62 for the definition of the bits in this register.

11.4.2 Command Register

This register contains the command code being sent to the device. Command execution begins immediately after this register is written. The command set is shown in Figure 69 on page 86.

All other registers required for the command must be set up before writing the Command Register.

11.4.3 Cylinder High Register

This register contains the high order bits of the starting cylinder address for any disk access. At the end of the command, this register is updated to reflect the current cylinder number.

In LBA Mode this register contains Bits 16–23. At the end of the command, this register is updated to reflect the current LBA Bits 16–23.

The cylinder number may be from zero to the number of cylinders minus one.

11.4.4 Cylinder Low Register

This register contains the low order 8 bits of the starting cylinder address for any disk access. At the end of the command this register is updated to reflect the current cylinder number.

In LBA Mode this register contains Bits 8–15. At the end of the command this register is updated to reflect the current LBA Bits 8–15.

The cylinder number may be from zero to the number of cylinders minus one.

11.4.5 Data Register

This register is used to transfer data blocks between the device data buffer and the host. It is also the register through which sector information is transferred on a FORMAT TRACK command, and configuration information is transferred on a IDENTIFY DEVICE command.

All data transfers are 16 bits wide except ECC byte transfers, which are 8 bits wide. Data transfers are PIO only.

The register contains valid data only when DRQ=1 in the Status Register.

11.4.6 Device Control Register

Device Control Register							
7	6	5	4	3	2	1	0
–	–	–	–	1	SRST	-IEN	0

Figure 50. Device Control Register

This register is used to control the CompactFlash Card interrupt request and to issue an ATA soft reset to the card. This register can be written even if the device is BUSY.

Bit Definitions	Description
SRST (RST)	Software Reset. The device is held reset when RST=1. Setting RST=0 re-enables the device.
-IEN	Interrupt Enable. When –IEN=0, and the device is selected, device interrupts to the host will be enabled. When –IEN=1, or the device is not selected, device interrupts to the host will be disabled.

Figure 51. Device Control Register bit definitions

11.4.7 Device Address Register

Device Address Register							
7	6	5	4	3	2	1	0
–	–WTG	–H3	–H2	–H1	–H0	–DS1	–DS0

Figure 52. Device Address Register

This register contains the inverted device select and head select addresses of the currently selected device.

Bit Definitions	Description
–WTG	–Write Gate. This bit is 0 when a write operation is in progress; otherwise it is 1
–H3, –H2, –H1, –H0	–Head Select. These bits are the one's complement of the binary coded address of the currently selected head. –H0 is the least significant bit
–DS1	–Drive Select 1. This bit is 0 when device 1 (slave) is selected; otherwise it is 1
–DS0	–Drive Select 0. This bit is 0 when device 0 (master) is selected; otherwise it is 1

Figure 53. Device Address Register bit definitions

11.4.8 Device/Head Register

Devic/Head Register							
7	6	5	4	3	2	1	0
1	L	1	DRV	HS3	HS2	HS1	HS0

Figure 54. Device/Head Register

This register contains the device and head numbers.

Bit Definitions	Description
L	Binary encoded address mode select. When L=0, addressing is by CHS mode. When L=1, addressing is by LBA mode.
DRV	Device. When DRV=0, device 0 (master) is selected. When DRV=1, device 1 (slave) is selected.
-HS3, -HS2, -HS1, -HS0	Head Select. These four fits indicate binary encoded address of the head. HS0 is the least significant bit. At command completion, these bits are updated to reflect the currently selected head. The head number may be from zero to the number of heads minus one. In LBA mode, these bits are updated to reflect the current LBA bits 24–27.

Figure 55. Device/Head Register bit definitions

11.4.9 Error Register

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDNF	0	ABRT	TK0NF	AMNF

Figure 56. Error Register

This register contains status from the last command executed by the device or a diagnostic code.

At the completion of any command with the exception of Execute Device Diagnostic, the contents of this register are always valid even if ERR=0 in the Status Register.

Bit Definitions	Description
BBK	Bad Block. BBK=1 indicates a Bad Block is detected.
UNC	Uncorrectable Data Error. UNC=1 indicates an uncorrectable data error has been encountered.
IDNF (IDN)	ID Not Found. IDNF=1 indicates the requested sector's ID field could not be found.
ABRT (ABT)	Aborted Command. ABT=1 indicates the requested command has been aborted due to a device status error or an invalid parameter in an output register.
TK0NF (T0N)	Track 0 Not Found. T0N=1 indicates track 0 was not found during a Recalibrate command.
AMNF (AMN)	Address Mark Not Found. AMN=1 indicates the data address mark has not been found after finding the correct ID field for the requested sector.

Figure 57. Error Register bit definitions

11.4.10 Feature Register

This register is command specific. This is used with ACCESS META DATA STORAGE command, SET FEATURES command and FORMAT UNIT command.

11.4.11 Sector Count Register

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the device. If the value in the register is set to 0, a count of 256 sectors is specified.

If the register is zero at command completion, the command was successful. If not successfully completed, the register contains the number of sectors which need to be transferred in order to complete the request.

The contents of the register are defined otherwise on some commands. These definitions are given in the command descriptions.

11.4.12 Sector Number Register

This register contains the starting sector number for any disk data access for the subsequent command. The sector number is from one to the maximum number of sectors per track.

In LBA mode this register contains Bits 0–7. At the end of the command this register is updated to reflect the current LBA Bits 0–7.

11.4.13 Status Register

Status Register							
7	6	5	4	3	2	1	0
BSY	DRDY	DF	DSC	DRQ	CORR	0	ERR

Figure 58. Status Register

This register contains the device status. The contents of this register are updated whenever an error occurs and at the completion of each command.

If the host reads this register when an interrupt is pending, it is considered to be the interrupt acknowledge. Any pending interrupt is cleared whenever this register is read. If BSY=1. mo other bits in the register are valid.

Bit Definitions	Description
BSY	Busy. BSY=1 whenever the device is accessing the registers. The host should not read or write any registers when BSY=1. If the host reads any register when BSY=1, the contents of the Status Register will be returned.
DRDY (RDY)	Device Ready. RDY=1 indicates that the device is capable of responding to a command. RDY will be set to 0 during power on until the device is ready to accept a command.
DF	Device Fault. DF=1 indicates that the device has detected a write fault condition. DF is set to 0 after the Status Register is ready by the host.
DSC	Device Seek Complete. DSC=1 indicates that a seek has completed and the device head is settled over a track. DSC is set to 0 by the device just before a seek begins. When an error occurs, this bit is not changed until the Status Register is ready by the host, at which time the bit again indicates the current seek complete status. When the device enters into or is in Standby mode, this bit is set by device in spite of not spinning up.
DRQ	Data Request. DRQ=1 indicates that the device is ready to transfer a word or byte of data between the host and the device. The host should not write the Command register when DRQ=1.
CORR (COR)	Corrected Data. Always 0.
ERR	ERR=1 indicates that an error occurred during execution of the previous command. The Error Register should be read to determine the error type. The device sets ERR=0 when the next command is received from the host.

Figure 59. Status Register bit definitions

12.0 General operational descriptions

12.1 Reset Response

There are three types of resets in a CompactFlash device: a power-on reset, a hardware reset, and a software reset. There is also a reset called PCMCIA soft reset, which uses bit 7 of Configuration Option Register. It is treated as a hard reset.

Type	Description
Power On Reset (POR)	A reset carried out upon device's every power up sequence
Hard Reset (Hardware Reset)	A reset initiated by a raising edge of RESET signal (in True IDE mode) A reset initiated by a falling edge of RESET signal (In PC Card mode)
Soft Reset (Software Reset)	A reset initiated by changing bit 2 (SRST) of Device Control Register as 0, 1 then 0
PCMCIA soft reset	A reset initiated by changing bit 7 (SRESET) of Configuration Option Register as 0, 1 then 0. It is equivalent to a hardware reset

Figure 60. Reset type

Description	POR	Hard Reset	Soft Reset
Aborting Host interface	–	0	0
Aborting Device operation	–	(1)	(1)
Initialization of hardware	0	0	X
Internal diagnostics	0	0	X
Initialization of task file registers (2)	0	0	0
Initialization of registers at attribute memory	0	0	X
DASP– handshake (3)	0	0	0
PDIAG– handshake (3)	0	0	0
Reverting programmed parameters to power-on default	0	0	(4)
• Logical geometry (number of cylinders/heads/sectors)			
• Multiple mode			
• Write cache			
• Read look-ahead			
• ECC bytes for Read Long and Write Long			
• Delayed Write			
• On-demand prefetch			
• Byte transfer mode (3)			
• PIO transfer mode			
• DMA transfer mode (3)			
• ABLE mode			
Reset Standby timer	0	0	X

Figure 61. Reset Response

Notes:

– - not applicable
O - executed
X - not executed

(1) If the device receives a reset during cached writing, the reset completes after cached writing completes
(2) Initialized value of task file registers are shown in figure 58 below
(3) True IDE mode only
(4) If the device has received Set Features with feature code CCh prior to a reset, setting is reverted to the power-on default

12.2 Register Initialization

After power on, hard reset, or software reset, the register values are initialized as shown in the following figure.

Register	Default Value
Error	Diagnostic Code
Sector Count	01h
Sector Number	01h
Cylinder Low	00h
Cylinder High	00h
Device/Head	00h
Status	50h
Alternate Status	50h

Figure 62. Default Register values

The meaning of the Error Register diagnostic codes resulting from power on, hard reset, or the EXECUTE DEVICE DIAGNOSTICS command are shown in the following figure.

Code	Description
01h	No error detected
02h	Formatter device error
03h	Sector buffer error
04h	ECC circuitry error
05h	Controller microprocessor error
8xh	Device 1 failed

Figure 63. Diagnostic codes

12.3 Diagnostic and Reset considerations

For each Reset and Execute Device Diagnostic, the Diagnostic is done as follows:

Power On Reset, Hard Reset

DASP- is read by Device 0 to determine if Device 1 is present. If Device 1 is present Device 0 shall read PDIAG- to determine when it is valid to clear the BSY bit and whether Device 1 has powered on or reset without error, otherwise Device 0 clears the BSY bit whenever it is ready to accept commands. Device 0 may assert DASP- to indicate device activity. If Device 1 is not present, Device 0 does not Assert DASP- at POR.

Soft Reset

If Device 1 is present Device 0 shall read PDIAG- to determine when it is valid to clear the BSY bit and whether Device 1 has reset without any errors, otherwise Device 0 shall simply reset and clear the BSY bit. DASP- is asserted by Device 0 (and Device 1 if it is present) in order to indicate device active.

Execute Device Diagnostic

If Device 1 is present, Device 0 shall read PDIAG- to determine when it is valid to clear the BSY bit and if Device 1 passed or failed the EXECUTE DEVICE DIAGNOSTICS command, otherwise Device 0 shall simply execute its diagnostics and then clear the BSY bit. DASP- is asserted by Device 0 (and Device 1 if it is present) in order to indicate the device is active.

In all the above cases: Power on, RESET-, Soft reset, and the EXECUTE DEVICE DIAGNOSTICS command the Device 0 Error register is shown in the following table.

Device 1 Present?	PDIAG- Asserted?	Device 0 Passed	Error Register
Yes	Yes	Yes	01h
Yes	Yes	No	0xh
Yes	No	Yes	81h
Yes	No	No	8xh
No	(not read)	Yes	01h
No	(not read)	No	0xh

Figure 64. Reset error register values

x indicates the appropriate Diagnostic Code for the Power on, RESET-, Soft reset, or Device Diagnostic error.

12.4 Power-off considerations

12.4.1 Load/Unload

The product will support a minimum of 300,000 normal load/unloads.

The Load/Unload is a functional mechanism of the drive. It is controlled by the drive microcode. Specifically, unloading of the heads is invoked by the commands:

Microcode revision: CSxICxx (where 'x' can be any character)

Command

Standby	*UL → Complete
Standby Immediate	*UL → Complete

Reset

Soft Reset	*UL → **Rdy
Hard Reset	*UL → **Rdy

* UL means unload
** Rdy means interface ready

Figure 65. A Device's behavior by ATA commands

The microcode revision is referred to in words 23–26 in Figure 82 on page 95. This is 8 characters in ASCII.

Load/Unload is also invoked as one of the idle modes of the drive.

The specified start/stop life of the product assumes that Load/Unload is operated normally, NOT in emergency mode.

12.4.2 Emergency unload

When the heads are still loaded, the microcode cannot operate when the drive power is interrupted. The normal 5 V power is unavailable to unload the heads. In this case a normal unload of the heads is not possible. However, the heads are unloaded by routing the back-EMF of the spinning motor to the voice coil. The actuator velocity is greater than the normal case and the unload process is inherently less controllable without a normal seek current profile.

An emergency unload is intended to be called for in rare situations. Because this operation is inherently uncontrolled it is more mechanically stressful than a normal unload.

A single emergency unload operation is more stressful than 100 normal unloads. The use of an emergency unload reduces the start/stop life of the drive at a rate at least 100X faster than that of normal unload and may damage the drive.

Warranty is void on a drive that has experienced 3,000 or more emergency unloads.

12.4.3 Required power-off sequence

Problems can occur on most drives when the power is removed at an arbitrary time. The following are some examples of arbitrary power-off occurrence:

- Data loss from the write buffer
- If the drive is writing a sector and a partially-written sector with an incorrect ECC block results. The sector contents are destroyed and reading the partially-written sector results in a hard error
- Depending on the design of the drive, the heads may possibly land in the data zone instead of the landing zone

You may then turn off the drive in the following order:

1. Issue a STANDBY IMMEDIATE command
2. Wait until Command Complete Status is returned (It may take up to 350 ms in typical case)
3. Terminate power to the drive

This power-down sequence should be followed for entry into any system power-down state, or system suspend state, or system hibernation state. In a robustly designed system, emergency unload is limited to rare instancess such as battery removal during operation.

12.5 Sector Addressing Mode

12.5.1 Logical CHS Addressing Mode

The logical CHS addressing is made up of three fields: the cylinder number, the head number, and the sector number. Sectors are numbered from 1 to the maximum value allowed by the current CHS translation mode and can not exceed 255 (0FFh). Heads are numbered from 0 to the maximum value allowed by the current CHS translation mode and can not exceed 15 (0Fh). Cylinders are numbered from 0 to the maximum value allowed by the current CHS translation mode and cannot exceed 65535 (0FFFFh).

When the host selects a CHS translation mode using the INITIALIZE DRIVE PARAMETERS command, the host requests the number of sectors per logical track and the number of heads per logical cylinder. In requested mode the device computes the number of logical cylinders available.

The current CHS translation mode, as well as the default CHS translation mode, is returned by the Identify Device Information as shown in figure 82 on page 97.

12.5.2 LBA Addressing Mode

Logical sectors on the device shall be linearly mapped with the first LBA addressed sector (sector 0) being the same sector as the first logical CHS addressed sector (cylinder 0, head 0, sector 1). Irrespective of the logical CHS translation mode currently in effect, the LBA address of a given logical sector does not change. The following is always true:

LBA = ((cylinder * heads_per_cylinder + heads) * sectors_per_track) + sector – 1

where heads_per_cylinder and sectors_per_track are the current translation mode values.

On LBA addressing mode, the LBA value is set to the following register:

Device/Head	←	LBA bits	27–24
Cylinder High	←	LBA bits	23–16
Cylinder Low	←	LBA bits	15–8
Sector Number	←	LBA bits	7–0

12.6 Power Management Feature

The power management feature set permits a host to modify the behavior in a manner which reduces the power required to operate. The power management feature set provides a set of commands and a timer that enables a device to implement low power consumption modes.

The drive implements the following set of functions:

1. A Standby timer
2. IDLE command
3. IDLE IMMEDIATE command
4. STANDBY command
5. STANDBY IMMEDIATE command

12.6.1 Power Modes

Standby Mode The device interface is capable of accepting commands, but as the media may not immediately accessible, there is a delay while waiting for the spindle to reach operating speed.

Idle Mode Refer to the section of Adaptive Battery Life Extender Feature.

Active Mode The device is in execution of a command or accessing the disk media with read look-ahead function or write cache function.

12.6.2 Power Management Commands

The CHECK POWER MODE command allows a host to determine if a device is currently in, going to, or leaving standby mode.

The IDLE and IDLE IMMEDIATE commands move a device to idle mode immediately from the active or standby modes. The IDLE command also sets the standby timer count and starts the standby timer.

The STANDBY and STANDBY IMMEDIATE commands move a device to standby mode immediately from the active or idle modes. The STANDBY command also sets the standby timer count.

12.6.3 STANDBY command completion timing

1. Confirm the completion of writing cached data in the buffer to media
2. Unload the heads on the ramp
3. Set the DRDY bit and DSC bit in Status Register
4. Set the INTRQ (completion of the command)
5. Activate the spindle break to stop the spindle motor
6. Wait until the spindle motor is stopped
7. Perform the post process

12.6.4 Standby timer

The standby timer provides a method for the device to automatically enter standby mode from either active or idle mode following a host programmed period of inactivity. If the device is in the active or idle mode the device waits for the specified time period and if no command is received, the device automatically enters the standby mode.

If the value of SECTOR COUNT register on IDLE command or STANDBY command is set to 00h, the device will automatically set the standby timer to 109 minutes.

12.6.5 Status

In the active, idle, and standby modes, the device must have RDY bit of the status register set. If BSY bit is not set, device must be ready to accept any command.

In sleep mode the device's interface is not active. A host must not attempt to read the device's status or issue commands to the device.

12.6.6 Interface Capability for Power Modes

Each power mode affects the physical interface as defined in the following figure:

Mode	BSY	RDY	Interface active	Media
Active	x	x	Yes	Active
Idle	0	1	Yes	Active
Standby	0	1	Yes	Inactive

Figure 66. Power conditions

Ready (RDY) is not a power condition. A device may post ready at the interface even though the media may not be accessible.

12.6.7 Initial Power Mode at Power On

After a power on or a hard reset the device goes to an IDLE mode or STANDBY mode depending on the option.

12.7 Advanced Power Management Feature

This feature provides power saving without performance degradation. The Adaptive Battery Life Extender 3 (ABLE-3) technology intelligently manages transition among power modes within the device by monitoring access patterns of the host.

This technology has three idle modes: Performance Idle mode, Active Idle mode, and Low Power Idle mode. The drive supports Performance Idle mode and Low Power Idle mode.

This feature allows the host to select an advanced power management level. The advanced power management level is a scale from the lowest power consumption setting of 01h to the maximum performance level of FEh. Device performance may increase with increasing advanced power management levels. Device power consumption may increase with increasing advanced power management levels. The advanced power management levels contain discrete bands, described in the section of SET FEATURE command in detail.

This feature set uses the following functions:

- A SET FEATURES subcommand to enable Advanced Power Management
- A SET FEATURES subcommand to disable Advanced Power Management

The Advanced Power Management feature is independent of the Standby timer setting. If both Advanced Power Management level and the Standby timer are set, the device will go to the Standby state when the timer times out or the device's Advanced Power Management algorithm indicates that it is time to enter the Standby state.

The IDENTIFY DEVICE response word 83, bit 3 indicates that Advanced Power Management feature is supported if set. Word 86, bit 3 indicates that Advanced Power Management is enabled if set.

Word 96, bits 7-0 contain the current Advanced Power Management level if Advanced Power Management is enabled.

12.7.1 Performance Idle mode

This mode is usually entered immediately after Active mode command processing is complete instead of conventional idle mode. In Performance Idle mode, all electronic components remain powered and full frequency servo remains operational. This provides instantaneous response to the next command. The duration of this mode is intelligently managed as the following describes.

12.7.2 Low Power Idle mode

Power consumption is 55–65% less than that of Performance Idle mode. The heads are unloaded onto the ramp. The spindle is still rotated at the full speed. Recovery time to the Active mode is about 300 ms.

12.7.3 Transition Time

The transition time is dynamically managed by the user's recent access pattern instead of using fixed access times. The ABLE-3 algorithm monitors the interval between commands instead of the command frequency of ABLE-2. The algorithm supposes that next command will come with the same command interval distribution as the previous access pattern. The algorithm calculates the expected average saving energy and response delay for next command in several transition time case based on this assumption. And it selects the most effective transition time with the condition that the calculated response delay is

shorter than the value calculated from the specified level by the SET FEATURE ENABLE ADAPTIVE POWER MANAGEMENT command.

The optimal time to enter Performance Idle mode is variable depending on the user's recent behavior. It is not possible to achieve the same level of Power savings with a fixed entry time into Performance Idle because every users data and access pattern is different. The optimum entry time changes over time.

The same algorithm works for entering into Low Power Idle mode and Standby mode, which consumes less power but requires more recovery time switching from this mode to Active mode.

12.8 Seek Overlap

The drive provides an accurate seek time measurement method. The SEEK command is usually used to measure the device seek time by accumulating execution time for a number of SEEK commands. With typical implementation of the SEEK command, this measurement must including the device and host command overhead. To eliminate this overhead, the drive overlaps the SEEK command as described below.

The first SEEK command completes before the actual seek operation is over. Then device can receive the next SEEK command from the host but actual seek operation for the next SEEK command starts right after the actual seek operation for the first SEEK command is completed. In other words, the execution of two SEEK commands overlaps excluding the actual seek operation.

With this overlap, total elapsed time for a number of SEEK commands is the total accumulated time for the actual seek operation plus one pre and post overhead. When the number of seeks is large, just this one overhead can be ignored.

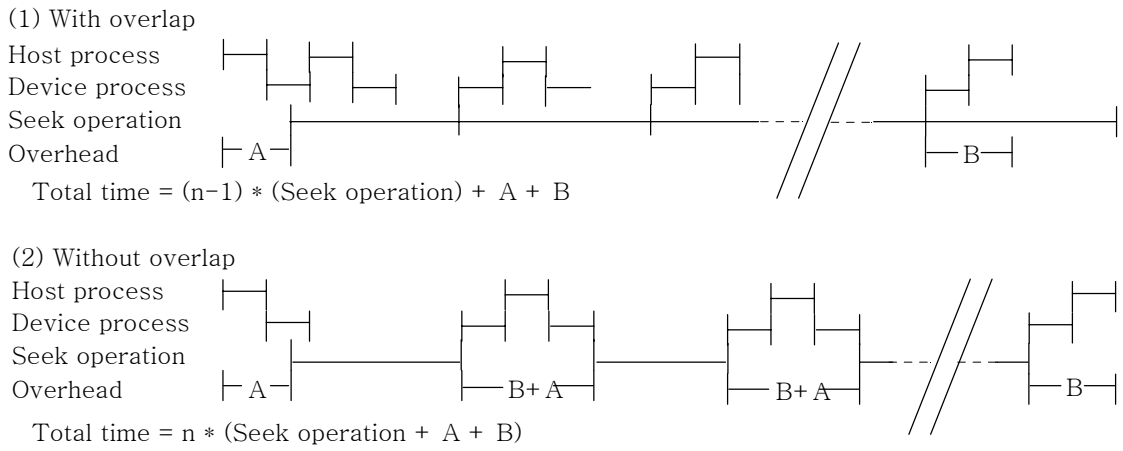

Figure 67. Seek overlap

12.9 Write Cache Function

Write cache is a performance enhancement whereby the device reports completion of the write command (WRITE SECTORS and WRITE MULTIPLE) to the host as soon as the device has received all of the data into its buffer. The device assumes responsibility for writing the data subsequently onto the disk.

- While writing data after a completed acknowledgment of a write command, a soft reset, or a hard reset does not affect its operation. However, a power off terminates the writing operation immediately and unwritten data gets lost.
- FLUSH CACHE, SOFT RESET, STANDBY, STANDBY IMMEDIATE and SLEEP are executed after the completion of a writing to disk media on enabling write cache function. So the host system can confirm the completion of the write cache operation by issuing FLUSH CACHE command, SOFT RESET, STANDBY command, and STANDBY IMMEDIATE command and then confirming the completion.
- The retry bit of WRITE SECTORS is ignored when write cache is enabled.

12.10 Delayed Write Function (Vendor Specific)

Delayed Write function is a power saving enhancement whereby the device delays the actual data writing into the media. When the device is in the power saving mode and the write command (WRITE SECTORS, WRITE MULTIPLE, or WRITE DMA) comes from the host, the transferred data is not written into the media immediately. The data is stored in the cache buffer. When the cache buffer becomes full, reaches a predefined size, or any command except the write command comes, the operation of writing the data from the cache buffer into the media begins.

The reason that the Delayed Write function reduces power consumption is as follows. When some write commands come with a long enough interval the device must exit the power saving mode and reenter the power saving mode again without a Delayed Write function. If the Delayed Write function is enabled then power saving mode transition times can be reduced. The additional energy for power saving mode transition is saved and then the average power consumption of the device is reduced.

The time duration from the write command completion until the media write completion is greatly extended with the Delayed Write function. If the power for the device is turned off during this time the data which has not been written to the media is lost. So a command listed in the Write Cache Function section is issued before the power off to confirm that the whole cached data has been written into the media.

For safety the Delayed Write function is disabled at the Power On Default. The ENABLE DELAYED WRITE command is issued to the device to enable Delayed Write function at every POWER ON RESET or HARD RESET. The actions of each reset are shown in Section 12.1 ATA Reset Response table on page 63.

12.10.1 ENABLE/DISABLE DELAYED WRITE command

The command code FAh with Feature register 07h enables the Delayed Write function.

The command code FAh with Feature register 87h disables the Delayed Write function.

Be careful that even if a Delayed Write function is enabled by command code FAh that a Delayed Write does not occur when the Write Cache function is disabled.

12.11 Reassign Function

The Reassign Function is used with read and write commands. The sectors of data for reassignment are prepared as the spare data sector. There are 448 spare sectors. One entry can register a maximum of 256 consecutive sectors.

This reassignment information is registered internally and the information is available upon completing the reassign function. The information is also used on the next power on reset or hard reset.

If the number of the spare sectors reaches 0, the reassign function will be disabled automatically.

The spare sectors for reassignment are located in a reserved area. As a result of reassignment the physical location of logically sequenced sectors is dispersed.

12.11.1 Auto Reassign Function

The sectors that show some errors may be reallocated automatically when specific conditions are met. The spare sectors for reallocation are located in the reserved area. The conditions for auto-reallocation are described below.

Nonrecovered write errors
When a write operation can not be completed after the Error Recovery Procedure (ERP) is fully carried out the sectors are reallocated to the spare location. An error is reported to the host system only when the write cache is disabled and the auto reallocation fails.

If the number of available spare sectors reaches 16 the write cache function is disabled automatically.

If the command is without retry and the write cache function is disabled the auto reassign function is not invoked.

Nonrecovered read errors
When a read operation fails after defined ERP is fully carried out a hard error is reported to the host system. This location is registered internally as a candidate for reallocation. When a registered location is specified as a target of a write operation, a sequence of media verification is performed automatically. When the result of this verification meets the criteria this sector is reallocated.

Recovered read errors
When a read operation for a sector failed once and then is recovered at the specific ERP step then this sector of data is reallocated automatically. A media verification sequence may be run prior to the relocation according to the predefined conditions.

12.12 Metadata Storage Function

Metadata storage is a small, nonvolatile user area which address space is logically separated from the main storage. The host can use metadata storage to store information on the data contents itself—for example, available free blocks, device properties, or any summary information. The first implementation of metadata storage in the drive provides just 32 bytes, however, the command set design does not preclude any future enhancement.

The metadata concept itself is not bound to any specific physical medium, although the drive's metadata storage has one important property for rotating devices: the host can access metadata without rotating the disk. This medium property is expected to supplement the applicability of the drive for digital appliances.

12.12.1 Metadata Storage Command Set

All metadata commands use command code B8h. Each command is specified as a subcommand of command B8h with Features Register containing the subcommand code. Cylinder Low and High registers are used to specify metadata block address into 512-byte units which ranges from 0 to [metadata capacity in bytes + 2] / 512. The drive provides 32 bytes of metadata capacity and the valid address for the drive is 0000h only. The Sector Count Register is used to specify the number of blocks transferred between the host and the device. The Sector Number Register is reserved and must be 00h for future use.

Inquiry Metadata Media, which uses subcommand code 02h, returns 1 sector of data containing information on the device's metadata storage. Read Metadata, which uses subcommand code 03h, can read metadata contents. Inquiry Metadata Media and Read Metadata return a status word that indicates whether the main storage contents have been modified since the last Write Metadata. The host can use the status word to check if metadata is not consistent with the main storage contents. Write Metadata, which uses subcommand code 04h, can write metadata. The device does not interpret metadata itself, though it is recommended that the first 10 bytes of metadata be a unique number that signifies the identity of the remaining data.

In addition to define new command set, Identify Device is enhanced to use word 161 as a capability bitstrap for CF command set extensions [which indicates support for the metadata command set].

Details of the command description are located in Section 13.5, "CF-ATA Command Description” on page 85.

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13.0 Command Protocol

The commands are grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined in the following text.

For all commands, the host must first check if BSY=1, and should proceed no further unless and until BSY=0. For all commands, the host must also wait for RDY=1 before proceeding.

A device must maintain either BSY=1 or DRQ=1 at all times until the command is completed. The INTRQ signal is used by the device to signal most, but not all, times when the BSY bit is changed from 1 to 0 during command execution.

A command shall only be interrupted with a hardware or software reset. The result of writing to the Command register while BSY=1 or DRQ=1 is unpredictable and may result in data corruption. A command should only be interrupted by a reset at times when the host thinks there may be a problem, such as a device that is no longer responding.

Interrupts are cleared when the host reads the Status Register, issues a reset, or writes to the Command Register.

13.1 Data In Commands

The Data In Commands include the following:

- Identify Device
- Read Buffer
- Read Long
- Read Multiple
- Read Sectors
- SMART Read Attribute Values
- SMART Read Attribute Thresholds

Execution includes the transfer of one or more 512 byte (>512 bytes on Read Long) sectors of data from the device to the host.

The following is a description of the execution process:

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head Registers.
2. The host writes the command code to the Command Register.
3. For each sector (or block) of data to be transferred:
   - The device sets BSY=1 and prepares for data transfer.
   - When a sector (or block) of data is available for transfer to the host, the device sets BSY=0, sets DRQ=1, and interrupts the host.
   - In response to the interrupt, the host reads the Status Register.
   - The device clears the interrupt in response to the Status Register being read.
   - The host reads one sector (or block) of data via the Data Register.
   - The device sets DRQ=0 after the sector (or block) has been transferred to the host.
4. For the Read Long command:
   - The device sets BSY=1 and prepares for data transfer.
   - When the sector of data is available for transfer to the host, the device sets BSY=0, sets DRQ=1, and interrupts the host.
   - In response to the interrupt, the host reads the Status Register.
   - The device clears the interrupt in response to the Status Register being read.
   - The host reads the sector of data including ECC bytes via the Data Register.
   - The device sets DRQ=0 after the sector has been transferred to the host.

The Read Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.

Note that the status data for a sector of data is available in the Status Register before the sector is transferred to the host.

If the device detects an invalid parameter, then it will abort the command by setting BSY=0, ERR=1, ABT=1, and interrupting the host.

If an error occurs, the device will set BSY=0, ERR=1, and DRQ=1. The device will then store the error status in the Error Register, and interrupt the host. The registers will contain the location of the sector in

error. The errored location will be reported with CHS mode or LBA mode, the mode is decided by mode select bit (bit 6) of Device/Head register on issuing the command.

If an Uncorrectable Data Error (UNC=1) occurs, the defective data will be transferred from the media to the sector buffer, and will be available to be transferred to the host, at the host's option. In case of Read Multiple command, the host should complete transfer the block which includes the error from the sector buffer and terminate whatever kind of type of error occurred.

All data transfers to the host through the Data Register are 16 bits with the exception of the ECC bytes, which are 8 bits.

13.2 Data Out Commands

These commands are

- Format Track
- Write Buffer
- Write Long
- Write Multiple
- Write Sectors
- Write Verify

Execution includes the transfer of one or more 512 byte (>512 bytes on Write Long) sectors of data from the host to the device.

The following is a description of the execution process:

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head Registers.
2. The host writes the command code to the Command Register.
3. The device sets BSY=1.
4. For each sector (or block) of data to be transferred:
   - The device sets BSY=0 and DRQ=1 when it is ready to receive a sector (or block).
   - The host writes one sector (or block) of data via the Data Register.
   - The device sets BSY=1 after it has received the sector (or block).
   - When the device has finished processing the sector (or block), it sets BSY=0, and interrupts the host.
   - In response to the interrupt, the host reads the Status Register.
   - The device clears the interrupt in response to the Status Register being read.
5. For the Write Long command:
   - The device sets BSY=0 and DRQ=1 when it is ready to receive a sector.
   - The host writes one sector of data including ECC bytes via the Data Register.
   - The device sets BSY=1 after it has received the sector.
   - After processing the sector of data the device sets BSY=0 and interrupts the host.
   - In response to the interrupt, the host reads the Status Register.
   - The device clears the interrupt in response to the Status Register being read.

The Write Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.

If the device detects an invalid parameter, then it will abort the command by setting BSY=0, ERR=1, ABT=1, and interrupting the host.

If an uncorrectable error occurs, the device will set BSY=0 and ERR=1, store the error status in the Error Register, and interrupt the host. The registers will contain the location of the sector in error. The erred location will be reported with CHS mode or LBA mode. The mode is decided by mode select bit (bit 6) of Device/Head register on issuing the command.

All data transfers to the device through the Data Register are 16 bits with the exception of the ECC bytes, which are 8 bits.

13.3 Non-Data Commands

These commands are as follows:

- Check Power Mode
- Enable/Disable Delayed Write
- Execute Device Diagnostic
- Flush Cache
- Format Unit
- Idle
- Idle Immediate
- Initialize Device Parameters
- Read Native Max ADDRESS
- Read Verify Sectors
- Recalibrate
- Seek
- Sense condition
- Set Features
- Set Max ADDRESS
- Set Multiple Mode
- Standby
- Standby Immediate

Execution of these commands involves no data transfer.

The following are the steps in the execution process:

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head Registers.
2. The host writes the command code to the Command Register.
3. The device sets BSY=1.
4. When the device has finished processing the command, it sets BSY=0, and interrupts the host.
5. In response to the interrupt, the host reads the Status Register.
6. The device clears the interrupt in response to the Status Register being read.

13.4 DMA Data Transfer Commands

The drive supports DMA Data Transfer Commands ONLY in True IDE mode. These commands are

- Read DMA
- Write DMA

Data transfer using DMA commands differ in the following two ways from PIO transfers:

- Data transfers are performed using the slave-DMA channel
- No intermediate sector interrupts are issued on multisector commands

Initiation of the DMA transfer commands is identical to the Read Sector or Write Sector commands except that the host initializes the slave-DMA channel prior to issuing the command.

The interrupt handler for DMA transfers differs in the following ways:

- no intermediate sector interrupts are issued on multisector commands
- the host resets the DMA channel prior to reading status from the device

The DMA protocol allows high performance multitasking operating systems to eliminate processor overhead associated with PIO transfers.

1. Host initializes the slave-DMA channel.
2. Host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder and Device/Head registers.
3. Host writes command code to the Command Register.
4. The device sets DMARQ when it is ready to transfer any part of the data.
5. Host transfers the data using the DMA transfer protocol currently in effect.
6. When all of the data has been transferred, the device generates an interrupt to the host.
7. Host resets the slave-DMA channel.
8. Host reads the Status Register and, optionally, the Error Register.

13.5 CF-ATA Command Description

This section defines the format of the commands the host sends to the drive. Commands are issued to the card by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command Register. The manner in which a command is accepted varies. There are three classes (see Table below) of command acceptance, all dependent on the host not issuing commands unless the card is not busy (BSY=0).

- Upon receipt of a Class 1 command, the card sets BSY within 400 ns.
- Upon receipt of a Class 2 command, the card sets BSY within 400 ns, sets up the sector buffer for a write operation, sets DRQ within 700 us, and clears BSY within 400 ns of setting DRQ.
- Upon receipt of a Class 3 command, the card sets BSY within 400 ns, sets up the sector buffer for a write operation, sets DRQ within 20 ms (assuming no reassignments), and clears BSY within 400 ns of setting DRQ.

Class	COMMAND	Code	FR	SC	SN	CY	DH	LBA
1	Access Metadata Storage	B8h	Y	Y	-	-	D	-
1	Check Power Mode	E5h or 98h	-	-	-	-	D	-
1	Execute Device Diagnostic	90h	-	-	-	-	D	-
1	Erase Sector(s)	C0h	-	Y	Y	Y	Y	Y
2	Format Track	50h	-	Y	Y	Y	Y	Y
1	Identify Device	ECh	-	-	-	-	D	-
1	Idle	E3h or 97h	-	Y	-	-	D	-
1	Idle Immediate	E1h or 95h	-	-	-	-	D	-
1	Initialize Device Parameters	91h	-	Y	-	-	Y	-
1	Read Buffer	E4h	-	-	-	-	D	-
1	Read DMA	C8h or C9h	-	Y	Y	Y	Y	Y
1	Read Long Sector	22h or 23h	-	-	Y	Y	Y	Y
1	Read Multiple	C4h	-	Y	Y	Y	Y	Y
1	Read Sector(s)	20h or 21h	-	Y	Y	Y	Y	Y
1	Read Verify Sector(s)	40h or 41h	-	Y	Y	Y	Y	Y
1	Recalibrate	1Xh	-	-	-	-	D	-
1	Request Sense	03h	-	-	-	-	D	-
1	Seek	7Xh	-	-	Y	Y	Y	Y
1	Sense Condition	F0h	Y	-	-	-	D	-
1	Set Features	EFh	Y	-	-	-	D	-
1	Set Multiple Mode	C6h	-	Y	-	-	D	-
1	Set Sleep Mode	E6h or 99h	-	-	-	-	D	-

Figure 68. CF-ATA Command Description (part 1 of 2)

Class	COMMAND	Code	FR	SC	SN	CY	DH	LBA
1	Standby	E2h or 96h	-	-	-	-	D	-
1	Standby Immediate	E0h or 94h	-	-	-	-	D	-
1	Translate Sector	87h	-	Y	Y	Y	Y	Y
1	Wear Level	F5h	-	-	-	-	Y	-
2	Write Buffer	E8h	-	-	-	-	D	-
2	Write DMA	CAh or CBh	-	Y	Y	Y	Y	Y
2	Write Long Sector	32h or 33h	-	-	Y	Y	Y	Y
3	Write Multiple	C5h	-	Y	Y	Y	Y	Y
3	Write Multiple w/o erase	CDh	-	Y	Y	Y	Y	Y
2	Write Sector(s)	30h or 31h	-	Y	Y	Y	Y	Y
2	Write Sector(s) w/o Erase	38h	-	Y	Y	Y	Y	Y
3	Write Verify	3Ch	-	Y	Y	Y	y	Y

Figure 69. CF-ATA Command Description (part 2 of 2

Definitions

FR = Features Register
SC = Sector Count Register
SN = Sector Number Register
CY = Cylinder Registers
DH = Card/Device/Head Register
LBA = Logical Block Address Mode Supported (see Section command descriptions for use)
Y - The register contains a valid parameter for this command. For the Device/Head Register Y means both the Card and head parameters are used
D - only the Card parameter is valid; the head parameter is not.

13.5.1 Access MetaData Storage - B8h

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	V	V	V	V	V	V	V	V
Sector Count	0	0	0	0	0	0	0	1
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	0	1	1	1	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	-	-	0	0	V

Figure 70. Access Metadata Storage Command (B8h)

This command accesses metadata storage area.

The following subcommands are supported and specified with Feature Register value.

Feature	Operation
02h	Inquiry Metadata Storage
03h	Read Metadata Storage
04h	Write Metadata Storage

Figure 71. Supported subcommand

Inquiry Metadata Storage (subcommand code - 02h) enables host to read capacity of the Metadata Storage of the device along with information associated with the charasteristics of the Metadata Storage. The data returned from the device is in following format.

word	data	Description
0	0001h	data format revision
1	0000h	media property bit 0: 1 = rotating, 0 = silicon bit 1-15: reserved
2	000xh	media status word bit 0: 1 = content changed 0 = content not changed bit 1-15: reserved
3	0020h	metadata capacity in bytes (low)
4	0000h	metadata capacity in bytes (high)
5	xxxxh	number of sectors per device(low)
6	xxxxh	number of sectors per device(high)
7 - 255	0000h	reserved

Figure 72. Data format of Inquiry Metadata Storage

Reserved bits and words are 0. Bit 0 of media status word (word 2) indicates whether the main storage contents have been changed by any commands (such as Write Sectors, Format Track, or Erase Sectors). Media status word is also returned by Read Metadata Storage as a header part of metadata.

Read Metadata Storage enables the host to read from device's metadata storage. Cylinder Low and Cylinder High Registers are used to specify the metadata block address, which can range from 0 to ([metadata capacity in bytes + 2] / 512). Sector Count Register is used to specify the number of sectors to transfer. For the microdrive, Cylinder Low and Cylinder High Registers must be 00h, Sector Count Register must be 01h because of the total capacity of metadata storage (32 bytes). The first block of metadata contains media status word that is also returned by Inquiry Metadata Media. Both words represent the identical information.

word	data	Description
0	000xh	media status word bit 0: 1 = content changed 0 = content not changed bit 1-15: reserved
1-32	xxxxh	metadata (32 bytes)
33-255	0000h	Reserved

Figure 73. Data format of Read Metadata Storage

Reserved words would be used if the device has more than 32 bytes of metadata capacity. The host should not assume capacity of metadata to be 32 bytes. The number is merely IBM Microdrive's implementation.

Write Metadata enables the host to write to the metadata storage of the device. Usage of Cylinder Low, Cylinder High and Sector Count Registers are the same as Read Metadata. Upon successful completion of Write Metadata, media status is reset to "unchanged" condition and subsequent media status word (by either Inquiry Metadata Media or Read Metadata) will show bit 0 cleared until the device receives any commands that changes the main storage contents.

The commands that affect media status are

- Write Sectors
- Write Sectors without Erase
- Write Long
- Write Verify
- Write Multiple
- Write Multiple without Erase
- Erase Sectors
- Format Track

Note: the list may grow if new commands are received that change the media contents.

word	data	description
0	xxxxh	ignored
1-32	xxxxh	metadata (32 bytes)
33-255	0000h	reserved

Figure 74. Data format of Write Metadata Storage

Word 0 is a pad and metadata starts with the word 1. Reserved words would be used if the device has more than 32 bytes of metadata capacity. The host should not assume capacity of metadata to be 32 bytes. The number is merely IBM Microdrive's implementation.

13.5.2 Check Power Mode (E5h/98h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -
Command	1 1 1 0 0 1 0 1

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	V V V V V V V V
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	- - - - - - - -
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	-	-	0	0	V

Figure 75. Check Power Mode Command (E5h/98h)

The Check Power Mode command will report whether the device is spun up and the media is available for immediate access.

Input Parameters From The Device

Sector Count The power mode code. The command returns FFh in the Sector Count Register if the spindle motor is at speed and the device is not in Standby or Sleep mode. Otherwise, the Sector Count Register will be set to 0.

13.5.3 Execute Device Diagnostic (90h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	1 - 1 - - - - -
Command	1 0 0 1 0 0 0 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	- - - - - - - -
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	V	V	V	V	V	V	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	-	-	0	0	0

Figure 76. Execute Device Diagnostic Command (90h)

The Execute Device Diagnostic command performs the internal diagnostic tests implemented by the device. The results of the test are stored in the Error Register.

The normal Error Register bit definitions do not apply to this command. Instead, the register contains a diagnostic code. Refer to Figure 63 on page 64 for the definition.

13.5.4 Erase Sectors (C0h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 77. Erase Sectors Command (C0h)

This command is implemented as a nop command with access range validation as the Hitachi Microdrive does not need pre-erase in advance of a write operation.

13.5.5 Flush Cache (E7h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -
Command	1 1 1 0 0 1 1 1

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	- - - - - - - -
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 78. Flush Cache Command (E7h)

This command causes the device to complete writing data from its cache.

The device returns a status, RDY=1 and DSC=1 (50h) in the following sequence:

1. Data in the write cache buffer is written to disk media
2. A successful completion is returned

13.5.6 Format Track (50h: Vendor Specific)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	1	0	1	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	0	V

Figure 79. Format Track (50h)

The Format Track command formats a single logical track on the device. Each good sector of data on the track will be initialized to zero with write operation. At this time, whether the sector of data is initialized correctly is not verified with read operation. Any data previously stored on the track will be lost.

The host transfers a sector of data containing a format table to the device. The format table should contain two bytes for each sector on the track to be formatted. The structure of format table is shown in Figure 80 page 95. The first byte should contain a descriptor value and the second byte should contain the sector number. The descriptor value should be 0 for a good sector, and any other descriptor value will cause an aborted error. The remaining bytes of the sector following the format table are ignored.

Since device performance is optimal at 1:1 interleave and the device uses relative block addressing internally, the device will always format a track in the same way no matter what sector numbering is specified in the format table.

Output Parameters To The Device

Sector Number	In LBA mode, this register specifies LBA address bits 0 - 7 to be formatted. (L=1)
Cylinder High/Low	The cylinder number of the track to be formatted. (L=0) In LBA mode, this register specifies LBA address bits 8 - 15 (Low), 16 - 23 (High) to be formatted. (L=1)
H	The head number of the track to be formatted. (L=0) In LBA mode, this register specifies LBA address bits 24 - 27 to be formatted. (L=1)

Input Parameters From The Device

Sector Number	In LBA mode, this register specifies current LBA address bits 0-7. (L=1)
Cylinder High/Low	In LBA mode, this register specifies current LBA address bits 8 - 15 (Low), 16 - 23 (High)
H	In LBA mode, this register specifies current LBA address bits 24 - 27. (L=1)
Error	The Error Register. An Abort error (ABT=1) will be returned under the following conditions: The descriptor value does not match the certain value. (except 00h)

In LBA mode, this command formats a single logical track including the specified LBA.

Explanation for descriptor

Descriptor : 00h	The sector of data will be initialized to 00h.

Byte	Data	Description
0	xxh	descriptor value for sector number 00h
1	00h	sector number
2	xxh	descriptor value for sector number 01h
3	01h	sector number
4	xxh	descriptor value for sector number 02h
5	02h	sector number
:	:	
N*2	xxh	descriptor value for sector number N
N*2+1	N	sector number (last sector for the track)
N*2+2	00h	remainder of buffer filled with 00h
N*2+3	00h	
:	:	
510	00h	
511	00h	

Descriptor : 00h - Format sector as good sector

Figure 80. Format track data field format

13.5.7 Identify Device (ECh)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -
Command	1 1 1 0 1 1 0 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	- - - - - - - -
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	0	V

Figure 81. Identify Device Command (ECh)

The Identify Device command requests the device to transfer configuration information to the host. The device will transfer a sector to the host containing the information in Figure 82 on page 97.

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848Ah	2	General configuration - signature for the CompactFlash Storage Card
1	0828h (0414h) (02B7h)	2	Default number of cylinders
2	0000h	2	Reserved
3	0010h	2	Default number of heads
6	003Fh	2	Default number of sectors per track
7-8	1D800020h (0EC00010h) (B090000Ah)	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
10-19	aaaa	20	Serial number in ASCII (Right justified)
22	0004h	2	# of ECC bytes passed on Read/Write Long Commands
23-26	aaaa	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word
47	8010h	2	Maximum number of sectors on Read/Write Multiple command
49	0F00h	2	Capabilities
51	0002h	2	PIO data transfer cycle timing mode
52	0001h	2	DMA data transfer cycle timing mode
53	0003h	2	Translation parameters are valid
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current number of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	2	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)
59	01XXh	2	Multiple sector setting
60-61	201D80h (100EC0h) (AB090h)	4	Total number of sectors addressable in LBA Mode
63	0203h	2	Multiword DMA Transfer Capability
64	0001h	2	Flow Control PIO Transfer modes supported
65	0096h	2	Minimum Multiword DMA Transfer Cycle Time
66	0096h	2	Manufacturer's Recommended Multiword DMA Transfer Cycle Time
68	00B4h	2	Minimum PIO Transfer Cycle Time with IORDY Flow Control
82	400C7068h	4	Command Set supported
84	4000h	2	Commad Set/Feature supported Extention
85	000C7044h	4	Command Set/Feature Enabled
87	4000h	2	Command Set/Feature Enabled
91	4060h	2	Current Advanced Power Management Level
129	0002h	2	Current Set Features Option, Bit Assignment
130	0005h	2	Reassigned Sectors
131	0001h	2	Initial Power mode Selection, Bit Assignment
132	0000h	2	User Signature
160	8100h	2	Power requirement description
161	8001h	2	CF command set Extentions

Figure 82. Word address and data field type information

General Configuration

This field informs the device is a CompactFlash Storage Card.

Default Number of Cylinders
This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

Default Number of Heads
This field contains the number of translated heads in the default translation mode.

Default Number of Sectors per Track
This field contains the number of sectors per track in the default translation mode.

Number of Sectors per Card
This field contains the number of sectors per card. This double word value is also the first invalid address in LBA translation mode.

Memory Card Serial Number
The contents of this field are right justified and padded with spaces (20h).

ECC Count
This field defines the number of ECC bytes used on each sector in the Read and Write Long commands.

Firmware Revision
This field contains the revision of the firmware for the Hitachi Microdrive.
Model Number
This field contains the model number for this product and is left justified and padded with spaces (20h).

Read/Write Multiple Sector Count
The even byte value of this field contains the maximum number of sectors that can be read or written per interrupt using the Read Multiple or Write Multiple commands.

Capabilities
Bit 13 = 0 : Standby timer operation is IBM specific
Bit 11 = 1 : IORDY supported
Bit 10 = 1 : IORDY can be disabled
Bit 9 = 1 : LBA mode supported
Bit 8 = 1 : DMA transfer supported (True IDE mode ONLY)

PIO Data Transfer Cycle Timing Mode
This field defines the mode for PIO data transfer.

DMA Data Transfer Cycle Timing Mode
This field defines the mode for DMA data transfer.

Translation Parameters are Valid
This field contains the value 0003h indicating that words 54 to 58 are valid and reflect the current number of cylinders, heads and sectors.

Current Number of Cylinders, Heads, Sectors/Track
These fields contains the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

Current Capacity
This field contains the product of the current cylinders times heads times sectors.

Multiple Sector Setting
This field contains a validity flag in the odd byte and the current number of sectors that can be transferred per interrupt for R/W Multiple in the even byte. The odd byte is always 01h, which indicates that the even byte is always valid.

The even byte value depends on the value set by the Set Multiple command. The even byte of this word by default contains a 00h, which indicates that R/W Multiple commands are not valid.

Total Sectors Addressable in LBA Mode
This field contains the number of sectors addressable for the card in LBA mode only.

Multiword DMA Transfer Capability
This field contains the capability of Multiword DMA Transfer. The low order byte identifies by bit all of the Modes which are supported, e.g., if Mode 0 is supported, bit 0 is set to one. The high order byte contains a single bit set to indicate which mode is active supported, e.g., if Mode 0 is active, bit 0 is set to one.

Flow Control PIO Transfer modes supported
Bits 7 through 0 of this field is defined as the Advanced PIO Data Transfer Supported Field. This field is bit significant. Any number of bits may be set in this field by the device to indicate which Advanced PIO Modes it is capable of supporting.

Of these bits, bits 7 through 2 are Reserved for future Advanced PIO Modes. Bit 0, if set, indicates that the device supports PIO Mode 3. Bit 1, if set, indicates that the device supports PIO Mode 4.

Note : For backwards compatibility with BIOS written before Word 64 was defined for advanced modes, a device reports in Word 51 the highest original PIO mode (that is, PIO mode 0, 1, or 2) it can support.

Minimum Multiword DMA Transfer Cycle Time
This field is defined as the Minimum Multiword DMA Transfer Cycle Time Per Word. This field defines, in nanoseconds, the minimum cycle time that the device can support when performing Multiword DMA transfers on a per word basis.

Manufacturer's Recommeded Multiword DMA Transfer Cycle Time
This field is defined as the Device Recommended Multiword DMA Transfer Cycle Time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector READ DMA or WRITE DMA command over all locations on the media under nominal conditions. If a host runs at a faster cycle rate by operating at a cycle time of less than this value, the device may negate DMARQ for flow control. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycle rate. Transfer at this rate does not ensure that flow control will not be used, but implies that higher performance may result.

Minimum PIO Transfer Cycle Time with IORDY Flow Control
This field is defined as the Minimum PIO Transfer With IORDY Flow Control Cycle Time. This field defines, in nanoseconds, the minimum cycle time that the device can support while performing data transfers while utilizing IORDY flow control.

Command Set Supported
Words 82, 83, and 84 indicate features/command sets supported. Bits 1 through 13 of word 83 and bits 0 through 13 of word 84 are reserved.

Bit 3 of word 82 is set to one, because Hitachi Microdrive supports the Power Management feature set.
Bit 5 of word 82 is set to one, because Hitachi Microdrive supports write cache.
Bit 6 of word 82 is set to one, because Hitachi Microdrive supports look-ahead.
Bit 12 of word 82 is set to one, because Hitachi Microdrive supports the Write Buffer command.
Bit 13 of word 82 is set to one, because Hitachi Microdrive supports the Read Buffer command.
Bit 14 of word 82 is set to one, because Hitachi Microdrive supports the NOP command.
Bit 2 of word 83 is set to one, because Hitachi Microdrive supports the CFA feature set.
Bit 3 of word 83 is set to one, because Hitachi Microdrive supports the Advanced Power Management feature set.

Command Set/Feature Enabled
Words 85, 86, and 87 indicate features/command sets enabled. Bits 1 through 15 of word 86 are reserved. Bits 0-13 of word 87 are reserved.

Bit 3 of word 85 is set to one, if the Power Management feature set has been enabled.

Bit 6 of word 85 is set to one, if the look-ahead has been enabled.
Bit 7 of word 85 is set to one, if the write cache has been enabled.
Bit 12 of word 85 is set to one, if the Write Buffer command has been enabled.
Bit 13 of word 85 is set to one, if the Read Buffer command has been enabled.
Bit 14 of word 85 is set to one, if the NOP command has been enabled.
Bit 2 of word 86 is set to one, if the CFA feature set has been enabled.
Bit 3 of word 86 is set to one, if the Advanced Power Management feature set has been enabled via the Set Features command.

Current Advanced Power Management Level
This field contains Current Value of Advanced Power Management Level.

Current Set Features Option, Bit Assignment
This field contains Current Option Value of Set Features.

Reassigned Sectors
This field contains the number of reassigned sectors.

Initial Power mode Selection, Bit Assignment
This field contains the mode definition at power on reset.

User Signature
This field contains user signature.

Power Requirement Description
This word is required for CompactFlash Storage Cards that support power mode 1.

Bit 15: VLD
if set to 1, indicates that this word contains a valid power requirement description.
if set to 0, indicates that this word does not contain a power requirement description.

Bit 14: RSV
This bit is reserved and must be 0.

Bit 13: -XP
if set to 1, indicates that the Card does not have Power Level 1 commands.
if set to 0, indicates that the Card has Power Level 1 commands

Bit 12: -XE
if set to 1, indicates that Power Level 1 commands are disabled..
if set to 0, indicates that Power Level 1 commands are enabled.

Bit 0-11: Maximum current
This field contains the Card's maximum current in mA.

CF Command Set Extentions
This word is assigned to have capability of CF command set extentions.

Bit 0:
If set to 1, indicates that Metadata command set is supported.
If set to 0, indicates that Metadata command set is not supported.

Bit 15:
If set to 1, Word 161 is valid.
If set to 0, Word 161 is not valid.

13.5.8 Idle (E3h/97h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	V V V V V V V V
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -
Command	1 1 1 0 0 0 1 1

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	- - - - - - - -
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 83. Idle Command (E3h/97h)

The Idle command causes the device to enter Idle mode immediatly, and set auto power down timeout parameter(standby timer). And then the timer starts counting down.

When the Idle mode is entered, the device is spun up to operating speed. If the device is already spinning, the spin up sequence is not executed.

During Idle mode the device is spinning and ready to respond to host commands immediately.

Output Parameters To The Device

Sector Count Timeout Parameter. If zero, the timeout interval (Standby Timer) is NOT disabled, but the timeout interval is set for 109 minutes automatically. If it is other than zero, the timeout interval is set for (Timeout Parameter x5) seconds.

The device will enter Standby mode automatically if the timeout interval expires with no device access from the host. The timeout interval will be reinitialized if there is a device access before the timeout interval expires.

13.5.9 Idle Immediate (E1h/95h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -
Command	1 1 1 0 0 0 0 1

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	- - - - - - - -
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 84. Idle Immediate Command (E1h/95h)

The Idle Immediate command causes the device to enter Idle mode.

The device is spun up to operating speed. If the device is already spinning, the spin up sequence is not executed.

During Idle mode the device is spinning and ready to respond to host commands immediately.

The Idle Immediate command will not affect the auto power down timeout parameter.

13.5.10 Initialize Device Parameters (91h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	H	H	H	H
Command	1	0	0	1	0	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	-	-	0	0	V

Figure 85. Initialize Device Parameters Command (91h)

The Initialize Device Parameters command enables the host to set the number of sectors per track and the number of heads minus 1, per cylinder. Words 54-58 in Identify Device Information reflects these parameters.

The parameters remain in effect until the following events take place:

- another Initialize Device Parameters command is received.
- the device is powered off.
- hard reset occurs.
- soft reset occurs and the Set Feature option of CCh is set

Output Parameters To The Device

Sector Count The number of sectors per track. 0 does not mean there are 256 sectors per track, but there is no sector per track.

H The number of heads minus 1 per cylinder. The minimum is 0 and the maximum is 15.

13.5.11 Read Buffer (E4h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -
Command	1 1 1 0 0 1 0 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	- - - - - - - -
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	0	V

Figure 86. Read Buffer Command (E4h)

The Read Buffer command transfers a sector of data from the sector buffer of device to the host.

The sector is transferred through the Data Register 16 bits at a time.

The sector transferred will be from the same part of the buffer written to by the last Write Buffer command. The contents of the sector may be different if any reads or writes have occurred since the Write Buffer command was issued.

13.5.12 Read DMA(C8h/C9h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	1 1 0 0 1 0 0 R

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	- - - - H H H H
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 87. Read DMA Command (C8h/C9h)

The Read DMA command reads one or more sectors of data from disk media, then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. The data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Output Parameters To The Device

Sector Count	The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
Sector Number	The sector number of the first sector to be transferred. (L=0) In LBA mode, this register specifies LBA address bits 0 - 7 to be transferred. (L=1)
Cylinder High/Low	The cylinder number of the first sector to be transferred. (L=0) In LBA mode, this register specifies LBA address bits 8 - 15 (Low) 16 - 23 (High) to be transferred. (L=1)
H	The head number of the first sector to be transferred. (L=0) In LBA mode, this register specifies LBA bits 24-27 to be transferred. (L=1)
R	The retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the sector to be transferred. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

13.5.13 Read Long (22h/23h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	0 0 0 0 0 0 0 1
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	0 0 1 0 0 0 1 R

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	- - - - - - - - V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	- - - - H H H H
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 88. Read Long Command (22h/23h)

The Read Long command reads the designated one sector of data and the ECC bytes from the disk media, then transfers the data and ECC bytes from the device to the host.

After 512 bytes of data have been transferred, the device will keep setting DRQ=1 to indicate that the device is ready to transfer the ECC bytes to the host. The data is transferred 16 bits at a time, and the ECC bytes are transferred 8 bits at a time. The number of ECC bytes are 4 or 40 according to the setting of the Set Feature option. The default setting is after power on is 4 bytes.

The command makes a single attempt to read the data and does not check the data using ECC. Whatever is read is returned to the host.

Output Parameters To The Device

Sector Count	The number of continuous sectors to be transferred. The Sector Count must be set to one.
Sector Number	The sector number of the sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 24-27. (L=1)
R	The retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred.
Sector Number	The sector number of the transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24-27. (L=1)

It should be noted that the device internally uses 40 bytes of ECC data on all data written or read from the disk. The 4-byte mode of operation is provided via an emulation. For testing the effectiveness and integrity of the ECC functions of the devide it is recommended that the 40-byte ECC mode should be used.

13.5.14 Read Multiple (C4h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	1 1 0 0 0 1 0 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	- - - - H H H H
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 89. Read Multiple Command (C4h)

The Read Multiple command reads one or more sectors of data from disk media, then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time. Command execution is identical to the Read Sectors command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector.

Output Parameters To The Device

Sector Count The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number The sector number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H The head number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 24 - 27. (L=1)

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8-15 (Low), 16-23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) LBA mode, this register contains current LBA bits 24 - 27. (L=1)

13.5.15 Read Sectors (20h/21h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	0 0 1 0 0 0 0 R

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	- - - - H H H H
Status	...See Below...

Error Register							
7 BBK	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	V	0	V	0	V	0	V

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	V	-	0	0	V

Figure 90. Read Sectors Command (20h/21h)

The Read Sectors command reads one or more sectors of data from disk media, then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Output Parameters To The Device

Sector Count	The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
Sector Number	The sector number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 24 - 27. (L=1)
R	The retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

13.5.16 Read Verify Sectors (40h/41h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	0 0 1 0 0 0 0 R

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	- - - - H H H H
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 91. Read Verify Sectors Command (40h/41h)

The Read Verify Sectors verifies one or more sectors on the device. No data is transferred to the host.

The difference of Read Sectors command and Read Verify Sectors command is whether the data is transferred to the host or not.

If an uncorrectable error occurs, the read verify will be terminated at the failing sector.

Output Parameters To The Device

Sector Count The number of continuous sectors to be verified. If zero is specified, then 256 sectors will be verified.

Sector Number The sector number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H The head number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 24 - 27. (L=1)

R The retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

Sector Count	The number of requested sectors not verified. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

13.5.17 Recalibrate (1Xh)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -
Command	0 0 0 1 - - - -

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	- - - - - - - -
Status	...See Below...

Error Register							
7 BBK	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	0	0	V	V	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	V	-	0	0	V

Figure 92. Recalibrate Command (1Xh)

The Recalibrate command moves the read/write heads from anywhere on the disk to cylinder 0.

If the device cannot reach cylinder 0, T0N (Track 0 Not Found) will be set in the Error Register.

13.5.18 Request Sense (03h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -
Command	0 0 0 1 - - - -

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	- - - - - - - -
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	V	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 93. Request Sense Command (03h)

This command requests extended error information for the previous command.

The following table defines the valid extended error codes for the Hitachi Microdrive. The extended error code is returned to the host in the Error Register.

Code	Error Type
00h	No Error Detected
09h	Miscellaneous Error
20h	Invalid Command
21h	Invalid Address (Requested Head or Sector Invalid)
2Fh	Address Overflow (Address Too Large)
11h	Uncorrectable ECC Error
05h	Self Test or Diagnostic Failed
10h	ID Not Found
3Ah	Spare Sectors Exhausted
0Ch	Corrupted Media Format
03h	Write/Erase Failed
22h	Extended Power Operations Disabled

Figure 94. Extended Error Codes

13.5.19 Seek (7Xh)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	- - - - - - - -
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	0 1 1 1 - - - -

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	- - - - - - - -
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	- - - - H H H H
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 95. Seek Command (7Xh)

The Seek command initiates a seek to the designated track and selects the designated head. The device need not be formatted for a seek to execute properly.

Output Parameters To The Device

Sector Number In LBA mode, this register specifies LBA address bits 0 - 7 for seek. (L=1)

Cylinder High/Low The cylinder number of the seek.
In LBA mode, this register specifies LBA address bits 8 - 15 (Low), 16 - 23 (High) for seek. (L=1)

H The head number of the seek.
In LBA mode, this register specifies LBA address bits 24 - 27 for seek. (L=1)

Input Parameters From The Device

Sector Number In LBA mode, this register contains current LBA bits 0 - 7. (L=1)

Cylinder High/Low In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

13.5.20 Sense Condition (F0h : vendor specific)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	0 0 0 0 0 0 0 1
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -
Command	1 1 1 1 0 0 0 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	V V V V V V V V
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	- - - D - - - -
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
V	V	0	V	-	-	0	V

Figure 96. Sense Condition Command (F0h)

The Sense Condition command is used to sense temperature in a device.

This command is executable without spinning up even if a device is started with No Spin Up option.

Output Parameters To The Device

Feature The Feature register must be set to 01h. All other value are rejected with setting ABORT bit in status register.

Input Parameters From The Device

Sector Count The Sector Count register contains result value.

Value	Description
00h	Temperature is equal to or lower than –20°C
01h-FEh	Temperature is (Value / 2 – 20)°C
FFh	Temperature is higher than 107°C

13.5.21 Set Features (EFh)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	V V V V V V V V
Sector Count	V V V V V V V V
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -
Command	1 1 1 0 1 1 1 1

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	- - - - - - - -
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	0	V

Figure 97. Set Features Command (EFh)

The Set Feature command establishes the following parameters which affect the execution of certain features as shown in the table below

ABT will be set to 1 in the Error Register if the Feature register contains any undefined values.

Feature	Operation
01h	Enable 8-bit data transfer
02h	Enable Write Cache
03h	Used for Set Transfer Mode command
05h	Set Advanced Power Management Mode
44h	Product specific ECC bytes (34 bytes) apply on Read/Write Long commands
55h	Disable Read Look Ahead
66h	Disable Power on Reset (POR) establishment of defaults at Soft Reset
69h	NOP n Accepted for backward compatibility
81h	Disable 8-bit data transfer
82h	Disable Write Cache
85h	Disable Advanced Power Management
96h	NOP n Accepted for backward compatibility
97h	Accepted for backward compatibility. Use of this feature is not recommended
9Ah	NOP n Accepted for backward compatibility
AAh	Enable Read Look Ahead
BBh	4 bytes of ECC apply on Read/Write Long commands
CCh	Enable Power on Rest (POR) establishment of defaults at Soft Reset

Figure 98. Features Supported

Features 01h and 81h are used to enable and clear 8-bit data transfer modes in True IDE Mode. If the 01h feature command is issued all data transfers will occur on the low order D7-D0 data bus and the IOIS16 signal will not be asserted for data register accesses.

Features 82h, AAh and BBh are the default features for the Hitachi Microdrive. Thus, the host does not have to issue this command with these features unless it is necessary for compatibility reasons.

Features 66h and CCh can be used to enable and disable whether the Power On Reset (POR) Defaults will be set when a soft reset occurs. The default setting is to revert to the POR defaults when a soft reset occurs.

Feature 05h is used for advanced power management. The Sector Count Register specifies the advanced power management level as below. The advanced power management level at power on reset is 60h.

- 80h - FEh Up to Low Power Idle mode
- 01h - 7Fh Up to Standby mode
- 00h, FFh Reserved

Feature 85h is used to disable advanced power management. This results in the same effect as the host uses features 05h with the Sector Count Register FEh.

13.5.22 Set Multiple (C6h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	V V V V V V V V
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -
Command	1 1 0 0 0 1 1 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	- - - - - - - -
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	0	V

Figure 99. Set Multiple Command (C6h)

The Set Multiple command enables the device to perform Read and Write Multiple commands and establishes the block size for these commands. The block size is the number of sectors to be transferred for each interrupt.

The default block size after power up, or hard reset is 0, and Read Multiple and Write Multiple commands are disabled.

If an invalid block size is specified, an Abort error will be returned to the host, and Read Multiple and Write Multiple commands will be disabled.

Output Parameters To The Device

Sector Count The block size to be used for Read Multiple and Write Multiple commands. Valid block sizes can be selected from 0, 1, 2, 4, 8 or 16. If 0 is specified, then Read Multiple and Write Multiple commands are disabled.

13.5.23 Standby (E2h/96h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	V V V V V V V V
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -
Command	1 1 1 0 0 0 1 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	- - - - - - - -
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 100. Standby Command (E2h/96h)

The Standby command causes the device to enter the Standby Mode immediately, and set the auto power down timeout parameter (standby timer).

When this command is issued, the device confirms the completion of the cached write commands before it asserts INTRQ. Then the device is spun down, but the interface remains active.

If the device is already spun down, the spin down sequence is not executed.

During the Standby mode the device will respond to commands, but there is a delay while waiting for the spindle to reach operating speed.

The timer starts counting down when the device returns to Idle mode.

Output Parameters To The Device

Sector Count Timeout Parameter. If zero, the timeout interval (Standby Timer) is NOT disabled, but the timeout interval is set to 109 minutes automatically. If other than zero, the timeout interval is set for (Timeout Parameter x5) seconds.

When the automatic power down sequence is enabled, the device will enter Standby mode automatically if the timeout interval expires with no device access from the host. The timeout interval will be reinitialized if there is a device access before the timeout interval expires.

13.5.24 Standby Immediate (E0h/94h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -
Command	1 1 1 0 0 0 0 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	- - - - - - - -
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 101. Standby Immediate Command (E0h/94h)

The Standby Immediate command causes the device to enter Standby mode immediately.

When this command is issued, the device confirms the completion of the cached write commands before asserts INTRQ. Then the device is spun down, but the interface remains active.

If the device is already spun down, the spin down sequence is not executed.

During the Standby mode the device responds to commands but there is a delay while waiting for the spindle to reach operating speed.

The Standby Immediate command will not affect the auto power down timeout parameter.

13.5.25 Translate Sector (87h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	- - - - - - - -
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	0 0 1 0 0 0 0 R

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	- - - - - - - -
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	- - - - H H H H
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 102. Translate Sector command (87h)

This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. The controller responds with a 512-byte buffer of information containing the desired cylinder, head and sector, including its Logical Address, and the Hot Count, if available, for that sector.

he following table represents the information in the buffer. Please note that this command is unique to the card.

Address	Information
00h-01h	Cylinder MSB (00), Cylinder LSB (01)
02h	Head
03h	Sector
04h-06h	LBA MSB (04) - LSB (06)
07h-12h	Reserved
13h	Erased Flag (FFh) = Erased; 00h = Not Erased
14h-17h	Reserved
18h-1Ah	Hot Count MSB (18) - LSB (1A)
1Bh-1FFh	Reserved

Figure 103. Translate Sector Information

13.5.26 Wear Level (F5h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	1 - 1 D V V V V
Command	1 1 1 1 0 1 0 1

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	0 0 0 0 0 0 0 0
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	- - - - - - - -
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 104. Wear Level Command (F5h)

This command is implemented as a nop command. However, the Sector Count Register is returned with 00h for backward compatibility.

13.5.27 Write Buffer (E8h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -
Command	1 1 1 0 1 0 0 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	- - - - - - - -
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	0	V

Figure 105. Write Buffer Command (E8h)

The Write Buffer command transfers a sector of data from the host to the sector buffer of the device. The sectors of data are transferred through the Data Register 16 bits at a time.

The Read Buffer and Write Buffer commands are synchronized such that sequential Write Buffer and Read Buffer commands access the same 512 byte within the buffer.

13.5.28 Write DMA (CAh/CBh)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	1 1 0 0 1 0 1 R

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	- - - - H H H H
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
V	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	0	V

Figure 106. Write DMA Command (CAh/CBh)

The Write DMA command transfers one or more sectors of data from the host to the device, then the data is written to the disk media.

The sectors of data are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. Data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Output Parameters To The Device

Sector Count	The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
Sector Number	The sector number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 24 - 27. (L=1)
R	The retry bit. If set to one, then retries are disabled. When write cache is enabled, They are ignored. (Ignoring the retry bit is in violation of ATA-3.)

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

13.5.29 Write Long (32h/33h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	0	0	0	0	0	0	0	1
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	0	1	1	0	0	1	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	0	V

Figure 107. Write Long Command (32h/33h)

The Write Long command transfers the data and the ECC bytes of the designated one sector from the host to the device, then the data and the ECC bytes are written to the disk media.

After 512 bytes of data have been transferred, the device will keep setting DRQ=1 to indicate that the device is ready to receive the ECC bytes from the host. The data is transferred 16 bits at a time, and the ECC bytes are transferred 8 bits at a time. The number of ECC bytes are 4 or 40 according to setting of Set Feature option. The default number after power on is 4 bytes.

Output Parameters To The Device

Sector Count The number of continuous sectors to be transferred. The Sector Count must be set to one.

Sector Number The sector number of the sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H The head number of the sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 24 - 27. (L=1)

R The retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred.
Sector Number	The sector number of the sector to be transferred. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the sector to be transferred. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the sector to be transferred. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

The drive internally uses 40 bytes of ECC on all data read or writes. The 4-byte mode of operation is provided via an emulation technique. As a consequence of this emulation it is recommended that a 40-byte ECC mode is used for all tests to confirm the operation of the files ECC hardware. Unexpected results may occur if such testing is performed using a 4-byte mode.

13.5.30 Write Multiple (C5h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	1 1 0 0 0 1 0 1

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	- - - - H H H H
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	0	V

Figure 108. Write Multiple Command (C5h)

The Write Multiple command transfers one or more sectors from the host to the device, then the data is written to the disk media.

Command execution is identical to the Write Sectors command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector. The sectors are transferred through the Data Register 16 bits at a time.

Output Parameters To The Device

Sector Count The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number The sector number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H The head number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 24 - 27. (L=1)

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

13.5.31 Write Multiple without Erase (CDh)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	0 0 1 1 0 0 0 R

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	- - - - H H H H
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	0	V

Figure 109. Write Multiple without Erase Command (CDh)

This command is identical to the Write Multiple command as the Hitachi Microdrive does not need pre-erase before a write operation.

13.5.32 Write Sector(s) (30h/31h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	0	1	1	0	0	0	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	0	V

Figure 110. Write Sector(s) Command (30h/31h)

The Write Sectors command transfers one or more sectors from the host to the device, then the data is written to the disk media.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the write will be terminated at the failing sector, when the auto reassign function is disable.

Output Parameters To The Device

Sector Count The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number The sector number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H The head number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 24 - 27. (L=1)

R The retry bit. If set to one, then retries are disabled. But ignored, when write cache is enabled. (Ignoring the retry bit is in violation of ATA-3.)

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0)In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

13.5.33 Write Sector(s) without Erase (38h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	0 0 1 1 0 0 0 R

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Error	...See Below...
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	- - - - H H H H
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	0	V

Figure 111. Write Sector(s) without Erase Command (38h)

This command is identical to the Write Sector(s) command as the Hitachi Microdrive does not need pre-erase before a write operation.

13.5.34 Write Verify (3Ch: Vendor Specific)

In DSCM-1xxxx implementation, the Write Verify command is exactly same as the Write Sectors command (30h). No read verification is performed after write operation.

Refer to Write Sectors Command for parameters.

13.6 Error Posting

The following table summarizes the valid status and error value for all the CF-ATA Command set.

V = valid on this command

	Error Register					Status Register				
COMMAND	BBK	UNC	IDNF	ABRT	AMNF	DRDY	DWF	DSC	CORR	ERR
Access Metadata Storage				V	V	V		V		V
Check Power Mode				V		V	V	V		V
Execute Device Diagnostic						V		V		V
Erase Sector(s)	V		V	V	V	V	V	V		V
Flush Cache			V	V	V	V		V		V
Format Track			V	V	V	V	V	V		V
Identify Device				V		V	V	V		V
Idle				V		V	V	V		V
Idle Immediate				V		V	V	V		V
Initialize Device Parameters						V		V		V
Read Buffer				V		V	V	V		V
Read DMA	V	V	V	V	V	V	V	V	V	V
Read Multiple	V	V	V	V	V	V	V	V	V	V
Read Long Sector	V		V	V	V	V	V	V		V
Read Sector(s)	V	V	V	V	V	V	V	V	V	V
Read Verify Sector(s)	V	V	V	V	V	V	V	V	V	V
Recalibrate				V		V	V	V		V
Request Sense				V		V		V		V
Seek			V	V		V	V	V		V
Sense Condition				V		V	V	V		V
Set Features				V		V	V	V		V
Set Multiple Mode				V		V	V	V		V
Set Sleep Mode				V		V	V	V		V
Standby				V		V	V	V		V
Standby Immediate				V		V	V	V		V
Translate Sector	V		V	V	V	V	V	V		V
Wear Level	V	V	V	V	V	V	V	V		V
Write Buffer				V		V	V	V		V
Write DMA	V		V	V	V	V	V	V		V
Write Long Sector	V		V	V		V	V	V		V
Write Multiple	V		V	V	V	V	V	V		V
Write Multiple w/o erase	V		V	V	V	V	V	V		V
Write Sector(s)	V		V	V	V	V	V	V		V
Write Sector(s) w/o Erase	V		V	V	V	V	V	V		V
Write Verify	V		V	V	V	V	V	V		V
Invalid Command Code				V		V	V	V		V

Figure 112. Error and Status Register

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14.0 Card information structure

00	01	CISTPL_DEVICE (5V Device Information Tuple)
02	03	Tuple length = 4 bytes
		Device Info fields
04	DB	Device ID
		Device Type (bit4..7) = D (DTYPE_FUNCSPEC)
		WPS (write protect switch) (bit3) = 1 (non WP)
		Device Speed (bit0..2) = 3 (DSPEED_150NS)
06	01	Device Size = 1 (2K bytes)
08	FF	End Mark
0A	1C	CISTPL_DEVICE_0C (Additional Device Information Tuple)
0C	04	Tuple length = 4 bytes
0E	03	Other Condition Info
		Ext (bit7) = 0
		Reserved (bit3..6) = 0
		Vcc Used (bit 1,2) = 1 (3.3V)
		MWAIT (bit0) = 1
		Device Info fields
10	DB	Device Information
		Device Type (bit4..7) = D (DTYPE_FUNCSPEC)
		WPS(write protect switch) (bit3) = 1 (non WP)
		Device Speed (bit0..2) = 3 (DSPEED_150NS)
12	01	Device Size Code = 1 (2K bytes)
14	FF	End Mark
16	18	CISTPL_JEDEC_C (JEDEC ID Tuple)
18	02	Tuple length = 2 bytes
1A	DF	PC Card ATA with no Vpp required for any operation
1C	01	
1E	20	CISTPL_MANFID (Manufacture ID Tuple)
20	04	Tuple length = 4 bytes
22	A4	TPLMID_MANF (Manufacture Code) = 00A4h for IBM
24	00	v
26	00	PLMID_CARD (Manufacture Info)

Figure 113. Card information structure

28	00	v
2A	15	CISTPL_VERS_1 (Level1 Version Tuple)
2C	12	Tuple length = 17h bytes
2E	04	Major Version = 4 (JEIDA 4.2/PCMCIA 2.1)
30	01	Minor Version = 1 v
32	"IBM"	
38	00	
3A	"microdrive"	
4E	00	
50	FF	End mark
52	21	CISTPL_FUNCID (Function ID Tuple)
54	02	Tuple length = 2 bytes
56	04	TPLFID_FUNCTION (IC Card function code) = 04 (Fixed Disk)
58	01	TPLFID_SYSINIT (System Initialization bit mask)
		POST(bit0) = 1
		ROM (bit1) = 0
5A	22	CISTPL_FUNCE (Function Extension Tuple)
5C	02	Tuple length = 2 bytes
5E	01	TPLFE_TYPE (Extension Type) = 01 (Disk Device Interface)
60	01	TPLFE_DATA (Interface Type) = 01 (PC Card ATA Interface)
62	22	CISTPL_FUNCE (Function Extension Tuple)
64	03	Tuple length = 3 bytes
66	02	TPLFE_TYPE (Extension Type) = 02 (Basic PC Card ATA Interface)
68	08	TPLFE_DATA
		V : Vpp[2::1] (bit0,1) = 00 (Vpp not required)
		S : Silicon (bit2) = 0 (Rotating device)
		U : Unique (bit3) = 1 (Model/Serial is unique)
		D : Dual drive (bit4) = 0 (single drive)
6A	0F	TPLFE_DATA
		P0 : Sleep (bit0) = 1 (support sleep mode)
		P1 : Standby (bit1) = 1 (support standby mode)
		P2 : Idle (bit2) = 1 (support idle mode)
		P3 : Auto (bit3) = 1(support automatic power control)
		N : 3F7/377 (bit4) = 0(include 3F7h 377h for I/O address)
		E : Index Emulate (bit5)= 0 (index emulation is not supported)
		I : IOIS16 (bit6) = 0
6C	1A	CISTPL_CONFIG (Configuration Tuple)

6E	05	Tuple length = 5 bytes
70	01	TPCC_SZ (Size of Fields Byte)
		TPCC_RASZ (Size of TPCC_RADR) (bit0,1) = 1 (2bytes)
		TPCC_RMSZ (Size of TPCC_RMSK) (bit2..5) = 0 (1byte)
72	07	TPCC_LAST (Last Entry Index) = 07
74	00	TPCC_RADR (Base address of Configuration Register) = 0200h
76	02	v
78	0F	TPCC_RMSK (Register Presence Mask) = 00001111b(200,202,204,206)
7A	1B	CISTPL_CFTABLE_ENTRY(16bit PCCardConfiguration Table Entry Tuple)
7C	0B	Tuple length = 0Bh bytes
7E	C0	TPCE_INDX (Configuration Table Index Byte)
		Config Entry Number (bit0..5)= 00 (Memory Mode)
		Default (bit6) = 1
		Interface (bit7) = 1 (interface field exist)
80	C0	TPCE_IF (Interface Description Field)
		Interface Type (bit0..3) = 00 (Memory)
		BVDs active (bit4) = 0
		WP active (bit5) = 0
		READY active (bit6) = 1
		M Wait required (bit7) = 1
82	A1	TPCE_FS (Feature Selection byte)
		Power (bit0,1) = 01 (Vcc only)
		Timing (bit2) = 0
		I/O (bit3) = 0
		Interrupt (bit4) = 0
		Memory (bit5,6) = 01
		Misc (bit7) = 1
		TPCE_PD (Power Description Structure)
84	27	Parameter Selection Byte
		NomV (bit0) = 1
		MinV (bit1) = 1
		MaxV (bit2) = 1
		PeakI (bit5) = 1
86	55	Power Parameter Definition (NomV)
		Exponent (bit0..2) = 5 (1V) --> 5.0 V
		Mantissa (bit3..6) = A (5.0)
88	4D	Power Parameter Definition (MinV)

		Exponent (bit0..2) = 5 (1V) --> 4.5 V
		Mantissa (bit3..6) = 9 (4.5)
8A	5D	Power Parameter Definition (MaxV)
		Exponent (bit0..2) = 5 (1V) --> 5.5 V
		Mantissa (bit3..6) = C (5.5)
8B	4E	Power Parameter Definition (PeakI)
		Exponent (bit0..2) = 6 (100mA) --> 450 mA
		Mantissa (bit3..6) = 9 (4.5)
		TPCE_MS (Memory Space Description Structure)
8C	08	Memory Space Descriptor Byte
		# of Windows (-1) (bit0..2) = 0 (# of window = 1)
		Length Size (bit3..4) = 1 (length field size = 1 byte)
		Card Address Size (bit5..6) = 0 (no card addr field)
		Host Addr (bit7) = 0 (arbitrary host addr)
8E	00	Window Descriptor
		Length of the window = 0
90	20	TPCE_MI (Miscellaneous Features Field)
		Max Twin Card (bit0..2) = 0
		Audio (bit3) = 0
		Read Only (bit4) = 0
		Power Down (bit5) = 1 (support power down mode)
92	1B	CISTPL_CFTABLE_ENTRY(16bit PCCard Configuration Table Entry Tuple)
94	06	Tuple length = 06h bytes
96	00	TPCE_INDX (Configuration Table Index Byte)
		Config Entry Number (bit0..5)= 00 (Memory Mode)
		Default (bit6) = 0
		Interface (bit7) = 0 (interface field exist)
98	01	TPCE_FS (Feature Selection byte)
		Power (bit0,1) = 01 (Vcc only)
		Timing (bit2) = 0
		I/O (bit3) = 0
		Interrupt (bit4) = 0
		Memory (bit5,6) = 00
		Misc (bit7) = 0
9A	21	Parameter Selection Byte
		NomV (bit0) = 1
		MinV (bit1) = 0

		MaxV (bit2) = 0
		PeakI (bit5) = 1
9C	B5	Power Parameter Definition (NomV)
		Exponent (bit0..2) = 5 (1V) --+-> 3.3 V
		Mantissa (bit3..6) = 6 (3.0) +
		Extension (bit7) = 1 (extension exists) +
9E	1E	Extension = 1Eh = +0.30 --+
A0	3E	Power Parameter Definition (PeakI)
		Exponent (bit0..2) = 6 (100mA) --> 350 mA
		Mantissa (bit3..6) = 7 (3.5)
A2	1B	CISTPL_CFTABLE_ENTRY(16bit PCCard Configuration Table Entry Tuple)
A4	0D	Tuple length = 0Dh bytes
A6	C1	TPCE_INDX (Configuration Table Index Byte)
		Config Entry Number (bit0..5)= 01 (I/O and Memory Mode)
		Default (bit6) = 1
		Interface (bit7) = 1 (interface field exist)
A8	41	TPCE_IF (Interface Description Field)
		Interface Type (bit0..3) = 01 (I/O and Memory)
		BVDs active (bit4) = 0
		WP active (bit5) = 0
		READY active (bit6) = 1
		M Wait required (bit7) = 0
AA	99	TPCE_FS (Feature Selection byte)
		Power (bit0,1) = 01 (Vcc only)
		Timing (bit2) = 0
		I/O (bit3) = 1
		Interrupt (bit4) = 1
		Memory (bit5,6) = 00
		Misc (bit7) = 1
		TPCE_PD (Power Description Structure)
AC	27	Parameter Selection Byte
		NomV (bit0) = 1
		MinV (bit1) = 1
		MaxV (bit2) = 1
		PeakI (bit5) = 1
AE	55	Power Parameter Definition (NomV)
		Exponent (bit0..2) = 5 (1V) → 5.0 V

		Mantissa (bit3..6) = A (5.0)
B0	4D	Power Parameter Definition (MinV)
		Mantissa (bit0..2) = 5 (1V) → 4.5 V
		Exponent (bit3..6) = 9 (4.5)
B2	5D	Power Parameter Definition (MaxV)
		Exponent (bit0..2) = 5 (1V) → 5.5 V
		Mantissa (bit3..6) = C (5.5)
B4	4E	Power Parameter Definition (PeakI)
		Exponent (bit0..2) = 6 (100mA) → 450 mA
		Mantissa (bit3..6) = 9 (4.5)
B6	64	TPCE_IO (I/O space address required for this configuration)
		IO Address Lines (bit0..4) = 4 (16byte boundary)
		Bus 16/8 (bit 5,6) = 3 (support 16/8 bit access)
		Range (bit 7) = 0
		TPCE_IR (Interrupt Request Description structure)
B8	F0	IRQ line 0..15 (bit0..3) = 0
		MASK (bit4) = 1
		Level (bit5) = 1
		Pulse (bit6) = 1
		Share (bit7) = 1
BA	FF	IRQ0..IRQ7 = all supported
BC	FF	IRQ8..IRQ15 = all supported
BE	20	TPCE_MI (Miscellaneous Features Field)
		Max Twin Card (bit0..2) = 0
		Audio (bit3) = 0
		Read Only (bit4) = 0
		Power Down (bit5) = 1 (support power down mode)
C0	1B	CISTPL_CFTABLE_ENTRY(16bit PCCard Configuration Table Entry Tuple)
C2	06	Tuple length = 06h bytes
C4	01	TPCE_INDX (Configuration Table Index Byte)
		Config Entry Number (bit0..5)= 01 (I/O and Memory Mode)
		Default (bit6) = 0
		Interface (bit7) = 0 (interface field exist)
C6	01	TPCE_FS (Feature Selection byte)
		Power (bit0,1) = 01 (Vcc only)
		Timing (bit2) = 0
		I/O (bit3) = 0

		Interrupt (bit4) = 0
		Memory (bit5,6) = 00
		Misc (bit7) = 0
		TPCE_PD (Power Description Structure)
C8	21	Parameter Selection Byte
		NomV (bit0) = 1
		MinV (bit1) = 0
		MaxV (bit2) = 0
		PeakI (bit5) = 1
CA	B5	Power Parameter Definition (NomV)
		Exponent (bit0..2) = 5 (1V) --+-> 3.3 V
		Mantissa (bit3..6) = 6 (3.0) +
		Extension (bit7) = 1 (extension exists) +
CC	1E	Extension = 1Eh = +0.30 --+
CE	3E	Power Parameter Definition (PeakI)
		Exponent (bit0..2) = 6 (100mA) --> 350 mA
		Mantissa (bit3..6) = 7 (3.5)
D0	1B	CISTPL_CFTABLE_ENTRY(16bit PCCard Configuration Table Entry Tuple)
D2	12	Tuple length = 12h bytes
D4	C2	TPCE_INDX (Configuration Table Index Byte)
		Config Entry Number (bit0..5)= 02 (I/O Primary Mode)
		Default (bit6) = 1
		Interface (bit7) = 1 (interface field exist)
D6	41	TPCE_IF (Interface Description Field)
		Interface Type (bit0..3) = 01 (I/O and Memory)
		BVDs active (bit4) = 0
		WP active (bit5) = 0
		READY active (bit6) = 1
		M Wait required (bit7) = 0
D8	99	TPCE_FS (Feature Selection byte)
		Power (bit0,1) = 01 (Vcc only)
		Timing (bit2) = 0
		I/O (bit3) = 1
		Interrupt (bit4) = 1
		Memory (bit5,6) = 00
		Misc (bit7) = 1
		TPCE_PD (Power Description Structure)

DA	27	Parameter Selection Byte
		NomV (bit0) = 1
		MinV (bit1) = 1
		MaxV (bit2) = 1
		PeakI (bit5) = 1
DC	55	Power Parameter Definition (NomV)
		Exponent (bit0..2) = 5 (1V) → 5.0 V
		Mantissa (bit3..6) = A (5.0)
DE	4D	Power Parameter Definition (MinV)
		Exponent (bit0..2) = 5 (1V) → 4.5 V
		Mantissa (bit3..6) = 9 (4.5)
E0	5D	Power Parameter Definition (MaxV)
		Exponent (bit0..2) = 5 (1V) → 5.5 V
		Mantissa (bit3..6) = C (5.5)
E2	4E	Power Parameter Definition (PeakI)
		Exponent (bit0..2) = 6 (100mA) → 450 mA
		Mantissa (bit3..6) = 9 (4.5)
E4	EA	TPCE_IO (I/O space address required for this configuration)
		IO Address Lines (bit0..4) = A (1Kbyte boundary)
		Bus 16/8 (bit 5,6) = 3 (support 16/8 bit access)
		Range (bit 7) = 1 (see range description)
E6	61	I/O range description byte
		# of address range -1 (bit0..3) = 1 (# of field = 2)
		size of address (bit 4,5) = 2 (2byte address)
		size of length (bit 6,7) = 1 (1byte length)
E8	F0	I/O address range description field #1 address = 1F0
EA	01	|
EC	07	V address block length = 8
EE	F6	I/O address range description field #2 address = 3F6
F0	03	|
F2	01	V address block length = 2
F4	EE	TPCE_IR (Interrupt Request Description structure)
		IRQ line 0..15 (bit0..3) = E ??
		MASK (bit4) = 0
		Level (bit5) = 1
		Pulse (bit6) = 1
		Share (bit7) = 1

F6	20	TPCE_MI (Miscellaneous Features Field)
		Max Twin Card (bit0..2) = 0
		Audio (bit3) = 0
		Read Only (bit4) = 0
		Power Down (bit5) = 1 (support power down mode)
F8	1B	CISTPL_CFTABLE_ENTRY(16bit PCCard Configuration Table Entry Tuple)
FA	06	Tuple length = 06h bytes
FC	02	TPCE_INDX (Configuration Table Index Byte)
		Config Entry Number (bit0..5)= 02 (I/O Primary Mode)
		Default (bit6) = 0
		Interface (bit7) = 0 (interface field exist)
FE	01	TPCE_FS (Feature Selection byte)
		Power (bit0,1) = 01 (Vcc only)
		Timing (bit2) = 0
		I/O (bit3) = 0
		Interrupt (bit4) = 0
		Memory (bit5,6) = 00
		Misc (bit7) = 0
		TPCE_PD (Power Description Structure)
100	21	Parameter Selection Byte
		NomV (bit0) = 1
		MinV (bit1) = 0
		MaxV (bit2) = 0
		PeakI (bit5) = 1
102	B5	Power Parameter Definition (NomV)
		Exponent (bit0..2) = 5 (1V) --+-> 3.3 V
		Mantissa (bit3..6) = 6 (3.0) +
		Extension (bit7) = 1 (extension exists) +
104	1E	Extension = 1Eh = +0.30 --+
108	3E	Power Parameter Definition (PeakI)
		Exponent (bit0..2) = 6 (100mA) --> 350 mA
		Mantissa (bit3..6) = 7 (3.5)
10A	1B	CISTPL_CFTABLE_ENTRY(16bit PCCard Configuration Table Entry Tuple)
10C	12	Tuple length = 12h bytes
10E	C3	TPCE_INDX (Configuration Table Index Byte)
		Config Entry Number (bit0..5)= 03 (I/O Secondary Mode)
		Default (bit6) = 1

		Interface (bit7) = 1 (interface field exist)
110	41	TPCE_IF (Interface Description Field)
		Interface Type (bit0..3) = 01 (I/O and Memory)
		BVDs active (bit4) = 0
		WP active (bit5) = 0
		READY active (bit6) = 1
		M Wait required (bit7) = 0
112	99	TPCE_FS (Feature Selection byte)
		Power (bit0,1) = 01 (Vcc only)
		Timing (bit2) = 0
		I/O (bit3) = 1
		Interrupt (bit4) = 1
		Memory (bit5,6) = 00
		Misc (bit7) = 1
		TPCE_PD (Power Description Structure)
114	27	Parameter Selection Byte
		NomV (bit0) = 1
		MinV (bit1) = 1
		MaxV (bit2) = 1
		PeakI (bit5) = 1
116	55	Power Parameter Definition (NomV)
		Exponent (bit0..2) = 5 (1V) → 5.0 V
		Mantissa (bit3..6) = A (5.0)
118	4D	Power Parameter Definition (MinV)
		Exponent (bit0..2) = 5 (1V) → 4.5 V
		Mantissa (bit3..6) = 9 (4.5)
11A	5D	Power Parameter Definition (MaxV)
		Exponent (bit0..2) = 5 (1V) → 5.5 V
		Mantissa (bit3..6) = C (5.5)
11C	4E	Power Parameter Definition (PeakI)
		Exponent (bit0..2) = 6 (100mA) → 450 mA
		Mantissa (bit3..6) = 9 (4.5)
11E	EA	TPCE_IO (I/O space address required for this configuration)
		IO Address Lines (bit0..4) = A (1Kbyte boundary)
		Bus 16/8 (bit 5,6) = 3 (support 16/8 bit access)
		Range (bit 7) = 1 (see range description)
120	61	I/O range description byte

		# of address range -1 (bit0..3) = 1 (# of field = 2)
		size of address (bit 4,5) = 2 (2byte address)
		size of length (bit 6,7) = 1 (1byte length)
122	70	I/O address range description field #1 address = 170
124	01	|
126	07	V address block length = 8
228	76	I/O address range description field #2 address = 376
12A	03	|
12C	01	V address block length = 2
12E	EE	TPCE_IR (Interrupt Request Description structure)
		IRQ line 0..15 (bit0..3) = E
		MASK (bit4) = 0
		Level (bit5) = 1
		Pulse (bit6) = 1
		Share (bit7) = 1
130	20	TPCE_MI (Miscellaneous Features Field)
		Max Twin Card (bit0..2) = 0
		Audio (bit3) = 0
		Read Only (bit4) = 0
		Power Down (bit5) = 1 (support power down mode)
132	1B	CISTPL_CFTABLE_ENTRY(16bit PCCard Configuration Table Entry Tuple)
134	06	Tuple length = 06h bytes
136	03	TPCE_INDX (Configuration Table Index Byte)
		Config Entry Number (bit0..5)= 03 (I/O Secondary Mode)
		Default (bit6) = 0
		Interface (bit7) = 0 (interface field exist)
138	01	TPCE_FS (Feature Selection byte)
		Power (bit0,1) = 01 (Vcc only)
		Timing (bit2) = 0
		I/O (bit3) = 0
		Interrupt (bit4) = 0
		Memory (bit5,6) = 00
		Misc (bit7) = 0
		TPCE_PD (Power Description Structure)
13A	21	Parameter Selection Byte
		NomV (bit0) = 1
		MinV (bit1) = 0

		MaxV (bit2) = 0
		PeakI (bit5) = 1
13C	B5	Power Parameter Definition (NomV)
		Exponent (bit0..2) = 5 (1V) --+-> 3.3 V
		Mantissa (bit3..6) = 6 (3.0) +
		Extension (bit7) = 1 (extension exists) +
13E	1E	Extension = 1Eh = +0.30 --+
140	3E	Power Parameter Definition (PeakI)
		Exponent (bit0..2) = 6 (100mA) → 350 mA
		Mantissa (bit3..6) = 7 (3.5)
142	14	CISTPL_NO_LINK (No Link Tuple)
144	00	Tuple length = 0 bytes
142	14	CISTPL_NO_LINK (No Link Tuple)
144	00	Tuple length = 0 bytes
146	FF	CISTPL_END (Tuple End)

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